Guest Editor's Introduction:  

The PowerPC in Perspective

Richard Mateosian

Why all the fuss about PowerPC? In my Micro Review column in this issue I review a book that goes into great detail on that point. I just want to add a few perspectives.

In his 1986 book, Marketing High Technology (ISBN 0-02-907990-X), Bill Davidow told the inside story of Intel's successful campaign to win the battle of the 16-bit microprocessors. We've all seen what a significant victory that was. Davidow posited an interesting rule of thumb. To challenge the market leader, you must spend an amount equal to about 70 percent of that leader's expected annual revenue. This is Davidow's estimate of the amount needed to overcome the barriers to entry.

I don't know how much IBM and Motorola have spent on the PowerPC, and I don't know Intel's projected revenues from the 486 and Pentium lines, but I can tell you that both numbers are pretty big. I think that's one of the reasons everyone is so interested.

Systems designers are excited for another reason. Glen Miranker and Jon Rubinstein, co-founders of PowerHouse Systems, explained to me that the implementation-based PC technology left them no flexibility to add value.

At the chip level, they felt that the PowerPC gave them good support for symmetric multiprocessing and provided the kind of floating-point performance that multimedia applications need. At the system level, they felt that the PowerPC Reference Platform would promote operating system compatibility, allowing them to differentiate their products without becoming nonstandard.

I know that IEEE Micro readers care about issues of architecture and implementation. PowerPC provides an interesting case study. At least two paths lead from the processors of the early 1990s to those of the late 1990s. Both paths involve issuing sequential instructions simultaneously. One path uses superpipelining and extremely fast clocks. The other exploits techniques of out-of-order and speculative execution. Neither path seems to depend much on the instruction set, so in that sense the war of hype between RISC and CISC is irrelevant.

PowerPC follows the path of out-of-order and speculative execution. Micro readers may remember an article about the Metaflow architecture that appeared in our June 1991 issue. That article discussed techniques of out-of-order and speculative execution that are similar to those used in the PowerPC. It provides excellent background for the articles in this issue.

I'm grateful to the many people at IBM and Motorola who worked hard to write the articles in this issue. I'm also grateful to the technical reviewers, who by policy must remain anonymous. Each of them undertook the difficult task of reviewing all four of these articles. And as always, Marie English and her tiny staff at Micro headquarters have performed their largely invisible but critical tasks with great skill and professionalism.

I hope you enjoy reading the articles in this special issue.

Richard Mateosian is a free-lance technical writer and computer systems consultant. He has worked in the computer industry as a programmer, systems designer, technical marketer, and author. He serves as vice president of the Berkeley Chapter of the Society for Technical Communication and writes Micro's Review column. Mateosian received a PhD degree in mathematics from the University of California at Berkeley.

Direct comments about this special issue to Richard Mateosian, 2919 Forest Avenue, Berkeley, CA 94705-1310; srm@c2.org.