Guest Editor's Introduction:
Toward a World Filled with Computers

Ken Sakamura
University of Tokyo

I t is my pleasure to present another East Asia issue, the first in two years. In my Guest Editor's Introduction of 1991 I noted some differences between the North American and Japanese microelectronics research and development scenes. The United States tended to emphasize high-powered applications such as superfast workstations and gigabit networks. In contrast, Japan gave more attention to the need for cost performance in home electronics and other consumer-oriented products.

That was two years ago. Today, however, that clear-cut distinction is changing. True, we still see continued competition over development of high-performance CPUs in the 100-MIPS-plus class for workstations and personal computers, with little regard for power consumption or chip size. At the same time, however, growing importance is being given around the world to microprocessors in the 10-MIPS range. These processors—which along with high performance feature low-power dissipation and small chip size—support embedded systems. We are seeing the appearance of high MIPS-per-watt microprocessors. Ever since the collapse of the Berlin Wall between East and West, emphasis has been shifting away from military technology toward civilian electronics markets. Even the United States is pouring new energy into embedded processors for portable systems and other consumer products. The applications for high-performance microprocessors are beginning to change dramatically.

In the TRON Project that we have been promoting over the last several years, we have continued to describe the future computer society as evolving along certain lines. We see the objects that surround us in our daily lives becoming increasingly embedded with computer chips, sensors, and actuators. These computerized objects then become linked by wired and wireless networks, forming distributed-processing systems in which the objects collaborate with each other. (See Figure 1.)

We are now well into the 1990s, and things are moving increasingly in the direction of our predicted scenario. Recently, terms like computer-augmented environment and ubiquitous computing seem to have become buzzwords in computer science. They describe an environment in which computers are used everywhere around us. This trend reflects the advances in development of the constituent technologies, such as small but high-performance sensors and displays, and high-performance sensors with low-power dissipation. It is becoming quite feasible to realize a world filled with computers.

In the next few years the world of microelectronics is likely to undergo great changes. The time has come to look ahead to applications for a world full of computers. With this background in mind, I describe recent microprocessor developments in Japan and, as in past issues, bring readers up to date on the TRON Project.

Japan's microprocessors

It is still true that most originally developed processors in Japan are designed for embedded system use. Japan has a number of general semiconductor manufacturers, including NEC, Toshiba, Hitachi, Fujitsu, and Mitsubishi Electric. But when it comes to microprocessors for workstations and personal computers, the manufacturers are limited to licensed production of the architectures of US companies (especially RISC chips). In view of the demand for RISC chips, none of the Japanese firms is developing its own original chip for
workstation or personal computer use. Moreover, they are hesitant to attempt developing chips compatible with the Intel x86 family because of the potential for legal trouble. The result is a further strengthening of the trend toward chips for embedded systems.

A boom in CPU development for low-power equipment persuaded Japanese manufacturers to develop original-architecture microprocessors (MPUs) and microcontrollers (MCUs). But up to now these were nearly all 4-, 8-, or 16-bit products. (In terms of quantity the 4-bit chips are most common.) Practically the only 32-bit chips to date have been the TRON-specification chips developed by six firms and the NEC V series.

Since last year however, 32-bit MPUs and MCUs aimed at large scale use in portable systems have increased. ARM and Hobbit are well known outside Japan. Since 1992 various firms in Japan have announced 32-bit chips with low-power consumption aimed at the portable equipment market. The chips typically perform at 10 to 20 MIPS (in terms of VAX MIPS; that is, VAX 11/780 performance on Dhrystone 1.1 or 2.1 benchmarks). Their power dissipates at under 500 mW; the CPU core size is less than 50 mm². Specific applications include highly portable personal information systems and game machines.

The instruction set architecture of these chips typically blends RISC and CISC approaches, and a 16-bit instruction format improves object code efficiency. In other words, rather than going all out for performance as a pure RISC, Japan’s manufacturers balance performance needs with the needs for small object code size and higher code density. Architecturally, the design is conservative, but applications of state-of-the-art technology realize the advantages of both RISC and CISC approaches.

It is this reworking of processor design that deserves our attention. Because of the emphasis on preserving past computer system investment, the companies have long been reluctant to depart from architectures like the IBM 370 or Intel x86. But in the case of processors for embedded systems, they have found it relatively easy to switch over to a new microprocessor design each time new equipment is introduced. When they compare the new designs to larger computer systems, they are less concerned about past investment. Makers of VCRs or copiers, for example, who are embedded-MPU users, care little about whether past software investment or yesterday’s object code will run on a new system. Their concern is for deriving the maximum cost performance available at a given point in time. Thus they can readily adopt a processor with a new architecture.

In the latter half of 1992, NEC’s V800 series and Hitachi’s SH7000 series were announced as low-power 32-bit microprocessors. Then in the first half of 1993, Toshiba’s TX2 and Mitsubishi’s M16 were announced as second-generation TRON-specification, low-power-consumption processors for embedded systems. Common to each of these products is that their manufacturers are making available TRON-specification real-time operating systems. Table 1, next page, outlines the features of each new processor.

High-performance microprocessor development continues as well. Japanese manufacturers are presently gearing up to market three high-performance processors with original designs. Currently under development are Hitachi’s Gmicro/500, Fujitsu’s µVP, and Mitsubishi’s Gmicro/400. The last of these is a high-speed, 32-bit processor for embedded systems that supports only integer calculations.
Table 1. The 32-bit, low-power-consumption processors in Japan.

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<th>Processor</th>
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| NEC V810                 | 32-bit, low-power-consumption microprocessor  
2.2V to 5V power supply; 15-MIPS performance at 5V and 25 MHz with 500-mW power dissipation and 40-mW power consumption at 2.2V and 10 MHz  
32 general registers of 32 bits each; support for both 16-bit and 32-bit instruction formats, for efficient object code density  
Bit-string manipulation instructions; single-precision floating-point operation instructions conforming to IEEE Std. 754  
0.8-μm CMOS technology; 240,000 transistors on a 7.7x7.7-mm chip; an on-chip 1-Kbyte instruction cache  
RX732 ITRON-specification real-time operating system  
16-bit external bus version (V805) available                                                                                                                                 |
| Hitachi SH7000 series    | 32-bit microcontroller family with on-chip DSP facility  
16-MIPS performance at 20 MHz with a 5V power supply  
On-chip, 16-bit hardware multiplier unit for (16 bits x 16 bits + 42 bits) 42-bit multiplication and accumulation operation performed in 100 ns to 150 ns  
500-mW power consumption, or 100 mW with a 3V power supply  
0.8-μm CMOS process with a CPU core integrating 38,500 transistors in an area of 6.58 mm²  
Model SH7032 with peripheral functions and on-chip memory integrates approximately 593,000 elements on a 10.78 x10.1-mm chip  
16 general registers; 16-bit fixed-instruction format  
μITRON-specification operating system available                                                                                                                                      |
| Toshiba TX2              | 32-bit, TRON-specification, low-power-consumption microprocessor  
Approximately 14-MIPS performance at 25 MHz (5V power supply), 1.7 times faster than the first-generation TX1  
1/10th power consumption cut during WAIT instruction execution  
16-bit instruction execution in one clock cycle  
Chip size one half that of the TX1                                                                                                                                                  |
| Mitsubishi M16          | TRON-specification microcontroller with 16-bit external bus and 32-bit internal bus  
4- to 5-MIPS average performance at 10-MHz operation (5V power supply)  
16-bit instruction execution in one clock cycle  
Typical configuration (M3100052FP) integrates 2 Kbytes of memory and peripheral functions                                                                                           |

These are the only general-purpose microprocessors with an original architecture. As mentioned earlier, other products are being developed that license the RISC architectures of US firms (Sparc, HP-PA, Alpha, MIPS).

**Hitachi Gmicro/500.** This 32-bit, TRON-specification microprocessor adopts a superscalar architecture that permits 130-MIPS performance at 66 MHz. When compared to Intel's 66-MHz Pentium, this chip dissipates only a third as much power, is a third smaller, and is 20 percent faster. Its designers used a 0.6-μm CMOS process.

How is it that the Gmicro/500 boasts performance surpassing Intel's Pentium? The answer lies in its being targeted mainly for embedded system use. Because of Intel's lock on the personal computer market, the Gmicro/500 had no other choice but to aim for use in embedded control systems. And the only way to win in the high-performance embedded system market was to focus on small chip size, low-power consumption, and high speed. In other words, its excellence is the result of its being aimed not at personal computer and workstation use but at embedded systems.
This microprocessor also, of course, runs an ITRON-specification operating system. In addition, designers are developing a BTTRON2 specification operating system for workstation use. The latter operating system supports a hypertext structure at the operating system level, as well as offering functions for multimedia support, multilingual processing, and distributed processing; it provides a compact kernel.

Fujitsu μVP. The μVP is a vector-processing-architecture coprocessor for direct connection to TRON-specification 32-bit microprocessors. At 50 MHz, 206-Milop single-precision speed, and 106-Milop double-precision speed, this 0.5-μm CMOS chip performs on a par with early supercomputers.

Separate articles on these two products appear elsewhere in this special issue. They are examples of how manufacturers continue to take up the challenge of developing a Japanese-original chip running an originally developed operating system, and are steadily making progress in implementing the goal.

There was a time when people thought the future belonged only to RISC and that CISC chips would disappear. But in Japan the emphasis is on object efficiency. For this reason a blend of RISC and CISC designs was sought. As a result, people have come to appreciate an architecture like that of the TRON-specification chips; new microprocessors implementing this architecture are being developed today. Some of the applications for which they are being used are high-performance numerical control machines and communication control processors. Then we have the μVP coprocessor with its vector-processing approach, a unique product that stands out among the peripheral chips designed for the TRON architecture. A single-board computer running the Gmicro/500 and μVP is said to achieve performance equivalent to that of a Cray 1 supercomputer, demonstrating amazing progress in microelectronics technology.

**TRON Project update**

The TRON Project is looking ahead to a world filled with computers. As I noted at the beginning of this piece, interest is beginning to focus on environments that are filled with computers everywhere you look. The TRON Project has constructed a pilot TRON-concept Intelligent House with around 1,000 built-in computer elements. We are about to begin construction of the first TRON-concept Intelligent Building that incorporates tens of thousands of computers.

What sets the TRON Project apart is its attempt to get a jump on the next computer age by considering what kinds of computer applications are likely to emerge, actually building such applications, and feeding back the results into the design of basic components such as microprocessors and operating systems.

Besides trying to determine the most suitable architecture for an age when the number of microchips in use is thousands or ten thousands of times greater than today, this project takes a comprehensive look at questions such as the following. What should computers be made to do? What should they not be made to do? What kinds of infrastructures are needed? What rules are necessary for data interchange? In these ways the project is planning and building information infrastructures for the future.

**From the TRON Intelligent House to the TRON Hyper-Intelligent Building.** We completed the TRON-concept Intelligent House experiment, conducted as an application project to get an advance look at the future, in the spring of 1993. At the same time we finished the basic design of the TRON Hyper-Intelligent Building, incorporating tens of thousands of computer elements, in preparation for the start of construction later this year. (See Figure 2, next page.)

The significance of this project is that a life-size model of a "computers everywhere" building will be built and put to actual use as a place of work. The building's computers will be able to locate people wherever they go and will fine-tune lighting (see Figure 3), temperature, and other environmental factors to personal preferences. The overall model is that described earlier of "intelligent objects" (ordinary objects containing microchips, sensors, and actuators) linked in wired or wireless networks that enable them to coordinate their actions. The component parts making up these networks are the results of fundamental research and development taking place in the TRON Project. In addition to the microprocessors used to control the intelligent objects, these important development results include real-time operating systems, highlevel data interchange protocol, and human-machine interface specifications.

**The importance of open architecture.** One of the vital requirements of a processor in intelligent objects is outstanding real-time performance. Important likewise are the ability to be used as an ASIC core, the possibility of applying the same architecture to a whole range of processors from lowpower-consumption models to high-end products, and the adoption of an open-architecture policy so that anyone is free to develop compatible microprocessors. When intelligent objects become networked in the tens of thousands or millions, it would be highly unlikely that all the component parts could be supplied by one corporation. In such an age, the basic architectures, operating system interfaces, data interchange protocols, and other basic technologies will have to be open to all as social infrastructure. Success is not possible under the dominance of any one company. I believe this open-system approach needs thoughtful consideration.

**Subprojects.** I have already touched on the status of the TRON-specification microprocessors. Other fundamental subprojects are currently under way.

**ITRON.** The ITRON-specification real-time operating systems for embedded systems have been implemented for most Japanese microcontrollers, and it has become a de facto industry standard. The ITRON standards continually undergo
improvements; the newest version called μTRON 3.0 offers network support. That is, we extended the specification to permit application to distributed systems connected in loosely coupled networks. When CPU nodes running μTRON 3.0 are networked, programmers can use ordinary system calls to manipulate tasks or semaphores in other nodes. Naturally, the specifications are open. Any interested readers can obtain copies of the English-language specifications via Internet's anonymous ftp utsun.s.u-tokyo.ac.jp; the directory is /TRON/ITRON/SPEC.

BTRON. When the ubiquitous computer age finally arrives, failure to standardize a human-machine interface (HMI) will invite confusion. The BTRON subproject is not limited to personal computers but deals with this interface in a much broader sense. The BTRON operating system specifications define a compact, highly efficient graphical user interface-based operating system designed for use even in light switches, of the kind adopted in the TRON-concept Intelligent House (see Figure 1). Compared to Microsoft Windows, it runs at high speed with minimal resources. (A workable system has been implemented around an i286 processor running at 16 MHz, with 4 Mbytes of memory and a floppy-disk drive.)

BTRON's fully multitasking operating system also supports a hypertext/hypermedia function at the system level. Since it would hardly be feasible to apply the GUI approach to all the switches around us, the TRON HMI specifications also describe non-GUIs, such as physical switches and handles (called SUD). Also specified in the BTRON subproject is the TAD (TRON application databus) high-level data interchange protocol for use among intelligent objects. This protocol is starting to be used in systems consisting of intelligent objects linked by a simple token-ring bus (a μBTRON-specification bus), for system operation and the like, to achieve a consistent operation environment.

CTRON. These specifications apply to operating systems used in communications systems and servers such as big telephone companies and private branch exchanges. In 1993 Tandem Computers announced a nonstop computer system running on a CTRON-based operating system.

TRON progress. As this summary should indicate, the TRON Project is proceeding at a steady pace, making its mark
as an original Japanese computer development project. The standards and specifications produced by the TRON Project are openly available to anyone by writing to TRON Association, Katsuta Building 5F, 5-39, Mita 1-chome, Minato-ku, Tokyo 108, Japan. (The contact address for North America is TRON Association US Liaison Office, PO Box 23990, Tempe, AZ 85285.) Moreover, the standards can be used freely, without licensing fees.

Since readers are especially interested in microprocessors, I have prepared articles in this special East Asia issue on two of the chips I’ve mentioned: the general purpose microprocessor Gmicro500 and the “single-chip supercomputer” μVP coprocessor. Many other unusual microprocessors are being developed in Japan, but of these I have chosen to present a high-speed fuzzy chip. I hope you enjoy reading these three articles.

References

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December’s feature articles explore the organizational and economic aspects of designing and constructing standards; those practical tools that help us make tools. Guest Editor Stephen L. Diamond comments, “Without formal or informal standards, we can create nothing except that which operates in isolation. Standards provide an interface, a means of communication that lets two disconnected and disparate things work together as one.” When they are developed correctly, standards provide this bridge.

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