Guest Editor's Introduction

"Hot" and "Cool" Chips

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The annual Hot Chips Symposium is always an interesting experience. For Hot Chips IV, the program committee (chaired by Dave Patterson and myself) once again had the pleasure (and difficulty) of selecting from too many interesting papers. The conference itself was a stimulating experience, bringing together a wide variety of people from both industry and academia.

For those not familiar with Hot Chips, a brief introduction might be helpful. Hot Chips tries to offer some windows on the future, from the near future—chips readers can now buy—to futures several years away from market. To maintain this future orientation, the program committee often selects descriptions of chips that are works in progress. Some such chips are clearly research chips not intended for market. Some turn out to be research chips, although they weren't intended to be! Such uncertainty is natural when looking at the future... so if you attend Hot Chips, please remember that not everything presented actually materializes. (Information on past symposia appears yearly in IEEE Micro, beginning with Hot Chips I in the April and June 1990 issues.)

Each year the symposium tries to present an interesting mixture of papers on chips that are really "hot," but in various different directions. Some hot chips really do run at high temperatures, and the program committee looks for several that stretch people's ideas of buildability. These may well be research prototypes.

Some hot chips are actually "cool"—their interest lies in their ability to pack even more performance and features into smaller and more power-efficient amounts of silicon. This category has become increasingly important.

Some hot chips are hot, not in temperature, but in terms of interest. Either they display instructive research directions, or they represent new generations of widely used chip families.

For this special issue of IEEE Micro, I was lucky to be able to obtain articles on the newest, high-end chips from three of the major general-purpose microprocessor families. By now, you may have seen systems based on these chips. The fourth article represents a research chip based on another major architecture. I specifically focused on high-end microprocessors to give you a good opportunity for comparison and contrast of different approaches to similar problems.

The first two articles describe aggressive implementations of existing instruction sets, one CISC, one RISC. Alpert and Avnon describe the Intel Pentium processor. This superscalar processor includes two integer pipelines and one floating-point pipeline, separate instruction and dual-ported data caches, and a branch target buffer. Many of these features are new to this architecture family, and the article analyzes the challenges of matching these features to the required architecture, especially in the area of floating point.
In the second article Asprey et al. describe the Hewlett-Packard PA7100 CPU, the current fastest HP PA RISC chip. Emphasized here are the various performance features in each of many areas of the design. You might particularly want to study the cache discussion, as HP now seems alone in choosing off-chip primary caches. It is well worth studying the reasoning.

Next McLellan describes a recent RISC architecture, Digital's Alpha AXP, and its first implementation, the 21064. This two-issue implementation emphasized high clock rates, with small on-chip caches and large off-chip secondary caches.

Finally we move forward from leading-edge, commercially available CPUs to a research project. Agarwal et al. describe Sparcle, a Sparc variation designed for research in large-scale multiprocessing. Its goal is not to build the fastest single CPU but to add mechanisms to tolerate longer memory latencies, support fine-grain parallelism, and improve interprocessor communication, all to improve large-scale multiprocessors. Thus, Sparcle illustrates solutions to the challenges of performance improvement, but in a direction orthogonal to that of the previous papers.

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HOT CHIPS V WILL TAKE PLACE August 8-10, 1993, at Stanford University in California. The program should be available about the time of this issue's printing. If you'd like more information, contact John Hennessy at (415) 725-3712 or jlh@vssop.stanford.edu.

I thank the authors, who came through with articles on time, and the many other people who worked on this issue, especially Marie English and Dick Price of IEEE Micro.

John R. Mashey is director, systems technology, at Silicon Graphics, Inc. He works in a wide and rapidly changing range of technical and marketing activities. He has also worked at Bell Laboratories on various Unix-related projects and later contributed to the design of most Mips R-series RISC chips.

Mashey holds a BS degree in mathematics, and MS and PhD degrees in computer science, all from Pennsylvania State University. He served as an ACM national lecturer for four years and a Usenix program chair, and cofounded the SPEC benchmarking group. He has given more than 400 public talks on Unix, the Programmer's Workbench, software engineering, benchmarking, and the RISC architecture. He is a member of the IEEE Computer Society and the Association of Computing Machinery.

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