The second article by Mike Johnson addresses the systems design and performance issues involved with AMD's new 29000 microprocessor. This streamlined instruction processor extends well-publicized RISC principles into its operating system and hardware environment. A significant portion of the Am29000 architecture is implemented to enhance instruction pipeline efficiency and to provide single-cycle execution. The author also describes an application of the large, on-chip register files that is implemented on chip to improve performance. Next, he gives a detailed account of the fixed-length instruction set. Also included is a discussion of the trade-offs involved in the design of an on-chip MMU and a three-bus channel architecture. Finally, a section on exceptions and error reporting describes the manner in which errors are handled during either instruction access or data access.

The third article, authored by David Perlmutter and Alan Yuen, focuses on the newly introduced Intel 80387 coprocessor chip. This FPU provides a configuration in which the coprocessor function is not integrated on chip. The 80386 microprocessor, for which this chip is designed, was introduced in the December 1985 issue of IEEE Micro. The 80387 interfaces to the 80386 as a slave coprocessor through 32-bit address and data buses. The authors describe the system interface, the instruction set, and its execution, timing, and exception handling. Finally, they give an example that illustrates the application of this chip into multiprocessing and distributed processing systems.

The high-performance, high-integration approach to microprocessor architecture will continue to dominate design for some time to come. However, beyond this, application-specific microprocessor architectures for artificial intelligence, signal processing, and communications may proliferate. 

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