processor outputs to be driven directly by a tester for the purposes of testing system hardware.

The test mode is also used in the implementation of master/slave checking. All Am29000 outputs have a comparator which compares the output of an enabled off-chip driver with the signal being supplied internally to the driver. If the output of the driver does not agree with the input, an error is signalled externally. No other action is taken; the external error signal can have any desired effect on the processor or system.

In a master/slave configuration, two Am29000's are connected in parallel, with outputs of the slave processor disabled by the test mode. In this configuration, the slave processor checks the outputs of the master processor against its own (disabled) outputs. The slave processor thus checks that both it and the master processor have consistent operation, providing a good degree of local reliability.

The Am29000 is, in many respects, a second-generation RISC. We have consistently found that the desired goals of performance and flexibility could be met with a simple, straightforward set of architectural features. These results have confirmed and extended those achieved for previous RISCs.

The performance of the Am29000 has significantly exceeded our initial expectations. By concentrating on the efficiency of the processor pipeline during design, we were able to take maximum advantage of a single-cycle instruction-execution rate.

References


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