S
ince their inception in the early 1970's, micro-
processors have changed drastically in every
imaginable way. The low-performance and
simplistic architectures of the seventies have evolved
into the complex, powerful engines of today. These
eengines exhibit almost all of the essential mainframe
attributes—except the price.

The need for higher and higher performance drives
today's microprocessor architectures to mimic that of
the mainframe. The popular approach among the
manufacturers has been to integrate critical peripheral
functions on chip to better emulate system-type
performance. Initial 32-bit architectures were
restricted by the available technology and package
pin counts. However with the advent of the sub-
micron geometries of the advanced CMOS processes,
today's 32-bit microprocessors pack an unprece-
dented number of functions onto a single chip.

Manufacturers unquestionably and unanimously em-
brace the on-chip memory management unit, or
MMU. Other functions such as instruction caches,
data caches, buffers, and floating-point blocks are
becoming popular choices of the designers for on-
chip integration.

The catalyst for this latest high-integration, high-
performance spree has been the systems houses
(DEC, AT&T, and Hewlett-Packard), each of whom
instigated mainframe architectures for their own pro-
prietary microprocessors. The general-purpose MPU
vendors such as Intel, Fairchild, National, Motorola,
and AMD have responded to the pressures and com-
petitions from these systems houses by introducing
new microprocessor chips that incorporate the ad-
vanced mainframe features.

The Japanese have been equally aggressive in their
new designs of high-performance microprocessors. 
NEC's V60 and V70 microprocessors use architectures
that include not only the MMU but also an

**THE NEW GENERATION OF MICROPROCESSORS**

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arithmetic floating-point unit on chip. Hitachi and
Fujitsu have collaborated to produce a family of mi-
croprocessors adapted to the TRON operating sys-
tem. These processors incorporate instruction
pipelines as well as instruction and stack caches. 
However, unlike NEC, their FPU function is off
chip.

The European manufacturer, Inmos, has begun to
ship an upgraded version of its RISC-based Trans-
puter, which contains an on-chip FPU, 4K of static
RAM, and four standard communications links.
Motorola's newly announced 68030 contains an
on-chip MMU. In addition it also integrates 256-byte
instruction and data caches. National Semiconductor's
current chip set, including the 32332, does not in-
tegrate an MMU and caches on chip. However, the
new 32532 to be announced later this year contains
on-board MMU and instruction and data caches.

In this special issue, three articles represent the high-
performance, high-integration trend for the new
generation of 32-bit microprocessors. Colin
Hunter's article describes the basic architecture and
configuration of the Fairchild Clipper microproces-
sor. The Clipper module is a three-chip set compris-
ing a CPU/FPU, instruction cache MMU, and data
cache MMU. The Clipper architecture, characterized
by dual 32-bit buses to cache memory (one for in-
suctions and one for data), essentially doubles the
memory bandwidth over the single-bus architectures.
Further bandwidth improvement is achieved by burst-
mode updating of the caches. Other critical features—
dual pipelining, error recovery and prevention—are
also incorporated. Dual pipelining involves concurrent
operations of the ALU and the FPU, while the error
prevention/recovery feature permits contention-free
operations and accurate handling of the exceptions.
The second article by Mike Johnson addresses the systems design and performance issues involved with AMD's new 29000 microprocessor. This streamlined instruction processor extends well-publicized RISC principles into its operating system and hardware environment. A significant portion of the Am29000 architecture is implemented to enhance instruction pipeline efficiency and to provide single-cycle execution. The author also describes an application of the large, on-chip register files that is implemented on chip to improve performance. Next, he gives a detailed account of the fixed-length instruction set. Also included is a discussion of the trade-offs involved in the design of an on-chip MMU and a three-bus channel architecture. Finally, a section on exceptions and error reporting describes the manner in which errors are handled during either instruction access or data access.

The third article, authored by David Perlmutter and Alan Yuen, focuses on the newly introduced Intel 80387 coprocessor chip. This FPU provides a configuration in which the coprocessor function is not integrated on chip. The 80386 microprocessor, for which this chip is designed, was introduced in the December 1985 issue of IEEE Micro. The 80387 interfaces to the 80386 as a slave coprocessor through 32-bit address and data buses. The authors describe the system interface, the instruction set, and its execution, timing, and exception handling. Finally, they give an example that illustrates the application of this chip into multiprocessing and distributed processing systems.

The high-performance, high-integration approach to microprocessor architecture will continue to dominate design for some time to come. However, beyond this, application-specific microprocessor architectures for artificial intelligence, signal processing, and communications may proliferate. 

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