


different parts that need to be stocked for manufacturing. In the M3-286 board, there are only six different random-logic devices (excluding buffers). 

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References

1. M. Di Manzo et al., "Modiac: A Modular Integrated Microprocessor System for Industrial Automation and Process Control," *Proc. 6th IFAC Workshop on Distributed Computer Control Systems*, May 20-22, 1985, Monterey, Calif.
2. *IEEE Project 802—Local Network Standards Committee, Draft B*, IEEE Computer Society, Oct. 1981.
3. J. F. Schoch et al., "Evolution of the Ethernet Local Computer Network," *Computer*, Vol. 15, No. 8, Aug. 1982, pp. 10-27.
4. W. Ansaldi et al., "Modosk: il nucleo di sistema operativo distribuito di un nodo della rete Modiac," *Automazione e Strumentazione*, May 1982, pp. 61-66.
5. *Introduction to MOS*, Olivetti tech. manual (code no. 4002130Q), Sept. 1982.
6. *IEEE Standard 796-1983, Microcomputer System Bus*, IEEE order no. CN928. (This is the Multibus standard.)
7. *IEEE Standard 696-1983, Interface Devices*, IEEE order no. CN927. (This is the S-100 bus standard.)
8. A. A. Allison, "Status Report on the P896 Backplane Bus," *IEEE Micro*, Vol. 1, No. 1, Feb. 1981, pp. 67-82.
9. D. del Corso et al., *M3 Bus Systems and TOMP Architectures*, Sottoprogetto P1, Progetto Finalizzato Informatica, Consiglio Nazionale delle Ricerche, Obiettivo MUMICRO, Sept. 1983.
10. *VMEbus Specification manual*, Pub. no. M68KVBS (D4), Motorola, Inc., Phoenix, Ariz., Oct. 1981.
11. R. A. Downing, "Fastbus—Details of Addressing and Bus Mastership," *IEEE Trans. Nuclear Science*, Vol. NS-26, No. 4, 1979, pp. 4525-4530.
12. "Single-Chip 8-bit Microcomputer," *Philips Handbook*, Pub. no. IC3-09-82, Part 3, Sept. 1982.
13. R. Fabry, "Capability-based Addressing," *Comm. ACM*, Vol. 17, No. 7, July 1974, pp. 403-412.
14. *iAPX 286 Hardware Reference Manual*, Pub. no. 210760-001, Intel Corp., Santa Clara, Calif., Mar. 1983.

15. *SBC 286/10ES Single-Board Computer Design Guide*, Rev. 2, Pub. no. 145439-001, Intel Corp., Santa Clara, Calif., Sept. 1982.
16. *Multibus II Bus Architecture, Specification Handbook*, Rev. B, Manual no. 146077, Intel Corp., Santa Clara, Calif., Nov. 1983.



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