**PURPOSE:**
Texas Instruments' TMS 320 signal processing microchip is the most powerful and cost effective processor of its kind. The $200 TMS 320, with programs residing in RAM or ROM, obviates the need for expensive development systems and thus facilitates economical creation of inexpensive, portable, low-power, "shirt pocket sized" signal processing systems having approximately the processing power of a $30,000 AP-1208. The real-time LPC vocoder-on-a-chip has become a reality, and other applications abound including speech recognition, speaker verification, and computer vision. Personal computers and robots of the near-future will surely employ such processing power. The course describes techniques for exploiting "general purpose" computer architectures so as to produce time-efficient DSP software. The TMS 320 micro is emphasized while the PDP-11 is used as the introductory machine (i.e., the TMS 320 can be viewed as a stripped down, speeded up PDP-11).

**INCLUDED IN THE COURSE:**
Tuition of US $525, includes lunches, refreshments, the 500-page book *DIGITAL SIGNAL PROCESSING SOFTWARE*, by L. Robert Morris, and a floppy disc (PDP-11 format) containing source files for all the software in the book (FORTRAN, PDP-11 and TMS 320 assembler) plus a MACRO-TMS 320 cross assembler which provides output for the TI TMS 320. (IBM & TI PC versions also available) The book-floppy package alone normally sells for $250.

**WHO SHOULD BENEFIT FROM THIS COURSE:**
Electrical engineers, computer scientists, or others who have a good understanding of DSP algorithms and their applications, and who need to know how to fully exploit the DSP capabilities of the simple, fast, and incredibly cost-effective technologies represented by the TI DSP chip in particular and the next generation of 16-bit micros incorporating array multipliers in general.

**THE INSTRUCTOR:**
L. Robert Morris, a Professor of Systems and Computer Engineering at Carleton University, Ottawa, Canada, has been active in the speech and DSP research areas for 17 years. He has published more than 20 DSP-related papers in theTransactions and Conference Proceedings of the IEEE ASSP Society, including descriptions of the first real-time minicomputer software speech synthesis (1972); the first hardware LPC speech synthesizer (1973); the autogen technique for automated generation of time-efficient DSP software (1976); and program analysis techniques which predict the relative performance of different DSP algorithms by utilizing data movement considerations implicit in the internal structure of the algorithm's computational kernel (1978). He wrote the IEEE PROGRAMS FOR DIGITAL SIGNAL PROCESSING book's radix-4 FORTRAN, FFT — the fastest known HLL DFT program — and is also co-author of MINICOMPUTER SYSTEMS, ORGANIZATION, PROGRAMMING, AND APPLICATIONS (PDP-11). Prentice-Hall, 1977, a best-selling text chosen as the Main Selection of two U.S. computer professionals' book clubs.

Robert Morris is an Associate Editor of IEEE MICRO and is President of DSPS Inc., who specialize in off-the-shelf time-efficient DSP programs for the PDP-11, VAX-11, MC68000, and TMS 320 architectures. He has actively programmed the TI chip for a year and has written numerous TMS 320 software modules, including a 540 usec, 64 complex point, autogen FFT.

**COURSE OUTLINE:**
- **Arithmetic Processing Requirements of DSP Algorithms:** Control vs. computation; indexing, pointers; accumulators. Case studies: DFT: (FFT, PFA, WFTA); autocorrelation in LPC: (Direct, PB); LPC matrix inversion: (Levinson, Le Roux-Gueguen); Speech synthesis in LPC: (Direct, lattice).
- **Architectures of GP Computers:** Overview of evolution: PDP-8, IBM 360, PDP-11, VAX-11, MC6000, NS16000, RISC I, TMS 320, PDP-11: Detailed architecture, DSP programming, and use of the macro concept for autogen software production. Programming considerations for i-11 cache, pipeline.
- **Algorithms and Architectures:** Components of computational kernels: Multiply/accumulate, inner product, load/addr/subtract/store (FFT, PFA, WFTA), complex multiply (3 mult/3 add; 4 mult/2 add). Loads and stores: the invisible enemy.
- **Structures for c(k):** In-line code, subroutines, threaded and knotted code. Time, space, and efficiency tradeoffs.
- **Structures for Indexing and Control:** Conventional control, Autogen. Program generation programs.
- **Compilers:** Interpreters, threaded code, in-line code, optimizing compilers, structuring HLL c(k)'s for compilers.
- **DSP Systems Programming:** Systems concepts: modular programming, theory, practice.
- **The TI TMS320:** Architecture: instruction set; address modes; page, pointer, and data manipulation. Arithmetic sequence programming: data and coefficient scaling; addressing and instruction ordering strategies; utilities. Modular programming: subroutines and argument passing, case branch, threaded code, interrupt service routines, memory overlays. Input/output. Data and coefficient scaling techniques. Time/space tradeoffs via autogen. DSP case studies: A/D, D/A, ulaw mapping, windowing. FFT butterfly, convolution, biquad filter, modems, square root, software sine & divide. LPC: limited-memory, 32-bit autocorrelation (3 usec for 200 point, 10 lag); L-G matrix inversion (300 usec for 10'th order); lattice speech synthesis (20 usec/point, 10'th order); pitch detection. Comparative performance: TI vs. NEC vs. J-11. Software development systems: Software emulators, MACRO-11 and MS-DOS cross assemblers; TI EVA board/host communication.
- **The Future:** General Purpose vs Special Purpose: Market and technological forces. Mostek MK68200, LSI VAX, IBM Josephson Micro, Fujitsu 11 nsec 16x16 multiplier, Toshiba GaAs 80 psec micro.

*One full day will be devoted to the TI TMS 320.*

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