Editor:

The article entitled "A Performance Comparison of Three Contemporary 16-bit Microprocessors" (April 1983) contained several technical mistakes. It is possible that if they had been corrected the conclusions might have been changed. Here are a few of the errors:

- The 68000 was said to require five clock cycles for a write operation. The correct number is four, the same as for a read operation.
- The performance of the 12.5-MHz 68000L12 was downgraded to 12 MHz, stretching the cycle time from 80 ns to 83.3 ns.
- The 8086 was incorrectly credited with 12-MHz performance.
- The Z8000 was incorrectly credited with 12-MHz performance.
- The article compared 16-bit addressing, so that the program and variables were limited to 64K. This seemed to be excessively restrictive now with 256K dynamic RAM chips available and Ada looming massively in the background. The 68000 is the only microprocessor of the three compared which supports unsegmented addressing beyond 64K boundaries.

All comparisons were performed on paper. While not all of the comparisons could have been performed on real hardware, a spot check could have exposed four of the five mistakes.

The Z8000 has been available for over three years and the 68000 for over two years, with industry consensus that the Z8000 is a nice CPU but not in the same league with the 68000. The availability of unsegmented addressing beyond 64K boundaries in the 68000 contributes heavily to that consensus. This should have suggested the possibility of problems with the paper calculations, which indicated that the Z8000 had the highest-performance addressing mechanism for high-level language.

The company with which I am associated has shipped over two hundred 68000-based products in the past nine months. Most of these run at 12.5 MHz with no wait states, using 100-ns static RAM.

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Author's reply:

Hal Hardenbergh points out that my article contains several technical mistakes. However, most of these so-called mistakes are a consequence of misinterpretation by Hardenbergh.

In order to do a fair comparison, I proposed that the three microprocessors are or will be available with a 4-
Hardenbergh suggests that the comparison is not fair, since addressing mechanisms are compared and the physical addressable range of the microprocessors is not taken into account. The concept of addressing mechanisms has nothing to do with the physical addressable range, as Hardenbergh suggests, but is a purely high-level language concept and influences the execution speed. Therefore, the Z8000 can have a better speed performance than the MC68000 even though the MC68000 has a much larger addressable range.

Hardenbergh is not very satisfied with a performance comparison on paper, as he calls it. However, the advantages of such a mathematical model are very clear:

- Performance can be determined without using actual hardware. This method is based on correct knowledge about the system and its environment. Such analytical methods have already been used for several problems and have been applied to processors for many years. The advantages of such models are their low cost and their ability to predict performance before the microprocessor has been produced, when it exists only in the design phase. As I pointed out in my article, my analytical results are consistent with those derived in other studies performed on actual hardware.

- Analytical models provide generality. This has the advantage that these models can be applied to all (existing and nonexistent) cases. When, for instance, a manufacturer decides to introduce a 15-MHz clock, the model can be used to predict the performance of such a variant.

I must admit that the actual 68000 requires four clock cycles to do a memory write instead of the five cycles specified for the preliminary 68000. I applied this new figure to my model and within a few minutes the new performance results were available. (This is another advantage of analytical performance evaluation.) The figure below shows the new relative performance of the Z8000 and MC68000. When we compare this figure with Figure 7a of the April article, we see that the influence of fast memory is nil and that of slow memory small. This fact is easily explained—D_w is influenced by m_w not for fast memory (Equation 10 in the April article) but only for slow memory. The same small change would be observed in all the figures of the April article in which the memory's influence on the MC68000 is described. The other figures, for which we assume fast memory, would remain unaltered.

I agree with Hardenbergh that the availability of unsegmented addressing beyond 64K boundaries in the 68000 contributes heavily to its success. However, my analytical speed performance evaluation, and other researchers’ results cited in my article, cannot be neglected. The designer must always make trade-offs among execution speed, addressing range, and other advantages and disadvantages.

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