of CISCs) created room for register windows—a key point in this discussion. Furthermore, the simplicity of control in RISC I rendered microprogramming unnecessary; this in turn eliminated the control loop—frequently the most critical timing path in microprogrammed machines—as the determining factor of the machine cycle. Moreover, any argument suggesting that instruction sets are not a primary performance factor is an argument for designing architectures that allow easy and efficient implementation—i.e., RISCs.

Virtual memory/protection. Our comparison of the six computers was somewhat unfair in that only the VAX provides a virtual address space that is larger than the physical address space. Given that RISC I doesn’t provide the same function, perhaps RISC I should be considered in another class. Furthermore, RISC I provides no protection.

What about adding virtual memory capability to RISC I? In a virtual memory system, we first must have restartable instructions. Restarting a machine with simple instructions and addressing modes is quite easy, and RISC I is restartable. By how much would a virtual memory capability slow RISC I down? To find an accurate answer to this question, we looked at solutions used by other microprocessors. National Semiconductor has announced the 16082, a memory management chip that has an address cache and that normally translates virtual addresses into physical addresses in 100 nanoseconds.\(^3\) If we put this chip in a system with a RISC I, it would add another 100 nanoseconds to every memory access. Memory is referenced every 400 nanoseconds in a 7.5-MHz RISC I, so such a combination would reduce RISC performance by 25 percent. Because 80 percent to 90 percent of memory references in RISC I are to instructions,\(^3\) more sophisticated approaches, such as translating addresses only when crossing a page boundary (as is done in the VAX-11/780) or providing a virtual address cache (as is done in the Dorado\(^4\)), would be needed to keep performance close to our goals.

Memory management subsumes protection. The most widely used computers rely on the separation of system and user states and associate protection with pages. If you believe this provides adequate security, then RISC I will suffice.

First silicon

The first RISC I was fabricated over the summer of 1981. The 44,500-transistor chip was designed in less time, with less manpower and fewer errors, than comparable CISC machines. Its original masks, for example, had only one design error. Programs first ran on a RISC I chip in the spring of 1982. Our first chips ran instructions at a clock rate of 1.5 MHz, considerably less than our projected 7.5 MHz. Even at that slow rate, however, RISC I ran programs faster than commercial microprocessors.\(^3\)

---

**UPGRADE YOUR AIM-65* INSTANTLY**

* A trademark of Rockwell Inc.

To A 6809 Development System

With The

"MACH-9"

From

M M S Inc.

**INTRODUCTORY PRICE**

$239.

Plus $6 U.P.S.

And Handling

Includes:

* 6809 CPU Plug-in Assembly
* Super-set of AIM Monitor
* Two-Pass Symbolic Assembler
* Complete Monitor Source Listings
* Enhanced Cut & Paste Editor
* 200 Page Manual
* Full I/O Control

"MACH-9" is assembled and tested with local BUS, 5 locking low force ROM sockets and 2K Static RAM

M M S Inc.

1110 E. Pennsylvania St.

TUCSON, AZ 85714

(602) 746-0418

Reader Service Number 4