requires the availability of the special hardware shown in
Figure 6.21
This special hardware includes two controlled right
shifters, X and Y registers, and two adder/subtractor cir-

cuits. The decision signals for the adder/subtractor are
generated by the sign bit of Y. Although Cordic is uni-
versally applicable to other elementary functions (sin, cos,
sinh, cosh, etc.), this characteristic is lost in typical
microprocessors unless their architecture has been ap-
propriately modified. This is mainly due to the scant shift
capability of microprocessors, which consists merely of a
single-bit-shift instruction set for single-word-length oper-
ands. The Cordic algorithm requires an instruction
repertoire with double-word-length shifts as well as multi-
ple-bit shifts. The double-word-length requirement is
necessary to maintain full machine precision, because in-
termediate computations must utilize $L + \log_2 L$ bits.21

Obviously desirable modifications include double-
word-length shift instructions and multiple-bit shift
capability, architectural revisions that should have a
significant impact on efficiency. However, Cordic can
implement several elementary functions with only minor
changes in the code. If several functions are required, less
code might be needed.21-23

Chen's algorithm

In an attempt to identify simple hardware for imple-
mentation of a unified algorithm on elementary func-

Figure 6. Special hardware configuration for Cordic
square root.

MANAGER,
DESIGN ENGINEERING

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