reading port A, and the second case in Table 3 outputs a short negative pulse upon writing port B. The last two cases in each table are manual low and high outputs. (Figure 7 shows a useful control-register programming form.)

The RT-level model presented in Table 1, when used with the manufacturer's timing data, enables the designer to analyze his hardware and software schemes for errors. Tracey points out that an RT structural-level description, such as that in Table 1, can be tedious. We assume, however, that the designer would use the table as a reference tool only, to help him analyze a particular operation or hook-up. Such a model should also be helpful to anyone needing to test a 6520.

Use of the model for analysis of interfacing schemes

The RT statements in Table 1 can serve as a tool for analyzing interfacing designs—here, we will discuss interfacing between a 6502 and a 6520, and between a 6520 and an external A/D converter.

6502-to-6520 interface. Consider, for example, the interfacing situation shown in Figure 8. The 6520 operation for this case can be obtained simply by substituting the 6502 outputs into the corresponding 6520 RT statements.

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