A Look at Variability and Aging

The need for more densely packed, faster and more energy-efficient devices has forced significant evolutions in device architectures in recent years. A challenging byproduct of such trends is increased variability of the performance parameters of manufactured devices and a move towards increased electrical stresses imposed on devices during their field use. In turn, increased electrical stress causes further increases in performance variability over time. In shorter form, two major obstacles arise for modern IC designers: variability and aging. The focus of this special issue is to bring to our attention the need for mediating impacts of variability and aging across the many stages of IC and integrated systems design. Developing innovative, yet feasible solutions for these matters are an urgent concern for future computing systems surging forward on the cusp of innovation. This month we bring you a collection of articles that thoroughly examine how the impacts of variability and aging are seen by experts and can be dealt with.

To begin this special-themed issue, a paper by Bowman et al. discusses the effects of variability on microprocessor performance through an analysis of error-detection and recovery circuits, among other circuit types and monitors. An article by Wang et al. then provides a detailed look at the variability and reliability of 6T SRAM memory systems, to show the criticality of variability effects on SRAM in computing systems. In our third article, Gupta and Roy continue the SRAM focus but specifically regard FinFET technology with a cost-benefit analysis through specific device and circuit co-design methods. Next, Chen et al. shed light on mitigating strategies to offset NBTI effects in current circuit optimizing methods. We follow this with a paper by Stott et al. that looks at the impacts of variability and aging in FPGAs. This article proposes an adaptive system that can reconfigure its own architecture to counter variability and aging effects. A sixth entry by Debashi and Fey presents the capabilities of using Boolean Satisfiability in automating speedpath debugging under timing variations.

We have also included in this final issue of 2013, three general interest articles that step away from our detailed look at variability and aging. The first of the three is an examination by Villacorta et al. of a dominant failure mechanism in nanometer technology—that of open defects in vias. Results of risk and reliability analyses show that new electromigration design rules are needed in light of resistive vias. The following article, provided by Laraba et al. from the TIMA Laboratory in Grenoble, demonstrates a low-cost digital monitoring alternative in reduced code testing. The last featured article is a contribution from Sayil et al. on transient noise effects caused by single event particles. The authors focus on coupling-induced soft-error mechanisms in combinational logic. We conclude this issue with “The Last Byte” by Scott Davidson.

We hope you enjoy reading this final issue of the year, and we look forward to bringing you relevant, thought-provoking, and informative articles in 2014. Already we have an exciting slate of issues to look forward to. From all of us who contribute to producing D&T issues, I would like to wish our readers a happy holiday season and express a big “thank you!” to all our authors and reviewers. See you all in 2014!

Andre Ivanov
Editor-in-Chief
IEEE Design & Test