Troubleshooting how and why circuits and systems fail is important and is rapidly growing in industry significance. Debug and diagnosis may be needed for yield improvement, process monitoring, correcting the design function, failure mode learning for research and development, or just getting a working first prototype. This detective work is, however, very tricky. Sources of difficulty include circuit and system complexity, packaging, limited physical access, shortened product creation cycle, and time to market. New and efficient solutions for debug and diagnosis have a much needed and highly visible impact on productivity.

This special section of IEEE Design & Test includes the extended versions of the three best contributions presented at the Silicon Debug and Diagnosis (SDD) Workshop, which was held in Anaheim, CA, USA, in November 2012. It was the eighth of a series of highly successful technical workshops that consider issues related to debug and diagnosis of semiconductor circuits and systems: from prototype bring-up to volume production.

The first paper, “Linking the verification and validation of complex integrated circuits through shared coverage metrics” by Hung et al., discusses how to bridge pre-implementation (commonly referred to also as “pre-silicon”) verification to post-implementation validation in an emulation environment. Considering the inherent flexibility offered by field-programmable gate arrays (FPGAs), the authors discuss how embedded instrumentation can aid data acquisition and coverage measurement in FPGA designs. The evolution of FPGA trace collection methods is elaborated, showing how recent tools can facilitate a set of predetermined cover points to be observed without requiring recompilation. Further, recent research is aimed at enabling any cover point to be measured in FPGA prototypes.

In the second paper, entitled “Evolution of graphics Northbridge test and debug architectures across four generations of AMD ASICs,” Margulis et al., present the evolution of the design for test and debug (commonly referred to as DFx) architectures over four generations of AMD designs. The paper covers different aspects of DFx, ranging from scan architecture to control (centralized, modular, hierarchical) to debug buses (asynchronous/synchronous, source synchronous). The key points are that DFx methodology must be physical-design friendly and account for high clock frequencies, needed to acquire and dump the trace data, as well as be aware of the power savings features, such clock and power gating.

In the last paper of this special section, entitled “Deriving feature fail rate from silicon volume diagnostics data,” Malik et al., address the challenge of identifying layout geometries that lead to systematic yield loss. As the subwavelength lithography gap continues to widen, this class of defect is becoming an increasingly dominant source of failures. With design-for-manufacturability (DFM) tools, it is possible to identify potential weaknesses in a design, but it remains extremely difficult to assess which DFM features will actually cause yield loss. The authors of this paper present a methodology to quantify the...
yield loss of DFM features using scan diagnosis data and finally separate the wheat from the chaff.

**We hope you** enjoy this subset of work that was initially presented at the 2012 SDD Workshop. This sample should give you some idea of the challenges that were addressed at the workshop and some of the most promising solutions. We are grateful to the authors who have taken the extra time to elaborate on their initial work so it could be shared with you here. As the challenges we face never seem to abate, information sharing within the industry continues to be one of the most important factors in moving our industry ahead. So, enjoy these excellent papers and then be sure to join us at the next SDD workshop.

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