A Look at Our Industry’s Challenges

**OUR INDUSTRY FACES** a complex myriad of potential problems and challenges across all mediums involving design and test, and the resulting solutions and research methods used to counter experience problems are even more varied and comprehensive. Thus, it makes sense for us at some point to introduce a variety of some of the most current and striking areas of contemporary research and experimentation to our readers. While a narrower focus on selected themes is certainly a top priority for us, the reality is that our industry is varied in the truest sense of the word, and the occasional wide-issue can serve immense benefits in representing this point.

This is what we have compiled in this issue; a compendium of recent, highly relevant selections that runs the gamut of problems and solutions in design and test, not only from an interindustry standpoint ranging from Trojans to 3D integration, but also from an international perspective that accounts for studies carried out across the globe. We have provided articles that should give our readers a highly interesting, yet widely informative, background on some of the most prevalent issues facing our global industry today. Indeed, our current market is filled with an ever-increasing need to go faster while maintaining fluid and efficient design; and this is a pursuit that must be highlighted on a cross-industry, global scope, if we are to fully take part in the increasing depth of international communication and collaboration.

To start things off, we follow up from our last issue’s focus by providing an examination of Trojan threats due to design vulnerability with “Protection Against Hardware Trojan Attacks: Towards a Comprehensive Solution.” A reliance on third-party hardware IP is also highlighted as a cause for concern. A protection solution is proposed to combine predeployment design with postdeployment monitoring—a comprehensive method with high hopes for future defense.

Our second entry, “Exploiting Multiple Mahalanobis Distance Metric to Screen Outliers From Analogue Product Manufacturing Test Responses,” provides an in-depth explanation from the University of Twente, The Netherlands, of two problems with the Mahalanobis Distance classification method, before suggesting a new, more effective method of Multiple Mahalanobis. The conclusions are exemplified by the study of a real-world automobile product.

A collaboration from New York University researchers is our third entry called “Expedited-Compact Architecture for Average Scan Power Reduction,” and proposes an architectural solution to strengthen the reliability of chip under test. This selection poses to minimize scan power hot spots and high heat, while upholding design flow and delivering savings in test power.

From here, we travel to researchers from the University of Ferhat Abbes in Algeria for our fourth entry, who present “An Optical BILBO for On-Line Testing of Embedded Systems,” an online optical testing approach to detect immediate faults in embedded systems without affecting normal operation. Using Built-In-Self-Test to combine duplication and comparison in real-time checking is examined, with the goal of stimulating further research on the benefits of optical testing.

Our fifth entry, “Automatic Calibration of Streaming Applications for Software Mapping Exploration,” proposes a tool flow that can efficiently map streaming applications onto an MPSoC virtual platform,
with a focus on timing annotation in sequential execution. A case study of an actual heterogeneous MPSoC is provided, to enforce the tool flow’s feasibility and the resulting accurate exploration of the virtual platform’s software mapping.

Our sixth entry, “XML-Based Hierarchical Description of 3D Systems and SIP,” compiled by researchers from the Fraunhofer Institute in Dresden, Germany, addresses smart product design. The opportunities in designing 3D-integrated electronic systems are shown to be influential in overcoming difficulties in exchanging data between EDA tools. The article extrapolates its findings and concludes with an impressive vision to adopt a standardized modeling language for tools needing geometry and material data.

We conclude with our seventh entry, “A Designer’s Guide to Subresolution Lithography: Enabling the Impossible to Get to the 14 nm Node,” an exciting and comprehensive discussion of past examples of double-patterning lithography, and how future uses of double-patterning can overcome harmful impacts on design, and defy the limits of optical lithography.

**We hope you** will enjoy, as much as we did, reading this compilation of articles addressing the challenges we face in design and test, and the potential solutions that are being offered.

Sincerely,

André Ivanov
Editor-in-Chief
*IEEE Design & Test*