The Quest for High-Yield IC Manufacturing

The past decade has seen steady scaling in process technology but no significant increase in time between the introduction of new technology generations. The semiconductor industry is now confronted with the problem that many failure mechanisms simply cannot be anticipated prior to manufacturing. Failures occur today because of complex interactions among physical design features that cannot be anticipated with test or monitor chips. As a result, there is a growing need to understand failures based on real products. Moreover, older methods of understanding failures based on physical failure analysis are no longer adequate, given the “nonvisual” natures of many defects, and the industry’s increasing reliance on diagnosis as a part of manufacturing bring-up. These drivers have led to significant progress in recent years in product-based yield learning, but a number of challenges still remain.

This timely issue introduces D&T readers to yield learning in this new era of manufacturing complexity, with emphasis on products as the vehicles for yield enhancement. Guest Editors Anne Gattiker and Phil Nigh have done an outstanding job in putting together this special issue with five selected articles, which include contributions by experts from both universities and industry. These articles cover the landscape of research advances, practical experiences, and perspectives on future trends. The first article, coauthored by experts from Mentor Graphics and Global Foundries, describes a framework for root-cause identification based on layout-aware diagnosis. The next article from Nvidia highlights the potential role that system-level test can play in reducing yield loss. The next three papers describe research breakthroughs in academia, with coverage of topics such as physically aware volume diagnosis, adaptive testing, and yield improvement for analog/mixed-signal circuits. The special issue also includes an enlightening perspectives article on yield learning from an industry veteran.

This issue of D&T includes a message to the readership from the newly formed D&T steering committee. Beginning 2012, D&T is being copublished by IEEE Council for Electronic Design Automation (CEDA), IEEE Circuits and Systems Society, IEEE Solid State Circuits Society and Test Technology Technical Council (TTTC). A steering committee with representatives from each of these four organizations has been constituted to guide D&T through this transition, and enhance the scope and content of the magazine in an appropriate manner. I am excited by the opportunities offered by the transition and I welcome the participation of the larger D&T community in this process.

I thank Anne and Phil for serving as Guest Editors of the special issue, the authors for their contributions, and the reviewers for their diligence and adherence to a tight review schedule, and I hope you will enjoy reading this special issue, as well as the subsequent issues of a revamped D&T in 2012. I wish all the D&T readers a very happy and successful new year!

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