Guest Editors’ Introduction: Asynchronous Design Is Here to Stay
(and Is More Mainstream Than You Thought)

Luciano Lavagno  
Politecnico di Torino

Montek Singh  
Univ. of North Carolina at Chapel Hill

**Asynchronous or clockless** design is poised to play a key role in alleviating fundamental challenges of current and future microelectronic circuits and systems. In particular, in order to maintain the continued growth in complexity of single chips, synchronous designers must increasingly contend with several challenges, including these:

- high-speed clock distribution,
- reducing power consumption,
- integration of multiple cores operating at different rates, and
- managing manufacturing and runtime variation.

Asynchronous design abandons clocking in favor of handshaking, thereby enhancing design modularity, reducing unnecessary switching activity, and accommodating delay variation. In fact, SoCs composed of multiple cores have already broken the single-clock paradigm; each chip typically has several distinct clock domains, and the overall integration is increasingly asynchronous (i.e., elastic) in nature.

Future computing technologies—including genetic, bio, nano, optical, and quantum—are expected to exhibit such high process variations that centralized control and synchronization are deemed unrealistic. Instead, an asynchronous approach, with its distributed control and natural elasticity, is likely to play an enabling role in making these emerging technologies feasible for building large-scale computing systems.

Asynchronous designers have recently given convincing demonstrations of its role in enabling high-speed as well as energy-efficient design, with several commercial products introduced to the market during the past decade. These products include gigahertz-rate FPGAs (Achronix Semiconductor), terabit-rate network switches (Fulcrum Microsystems), and low-power processors for use in electronic passports, pagers, and smartcards (Philips/Handshake Solutions).

This special issue of *IEEE Design & Test* presents seven articles that highlight recent advances in the field of asynchronous design, its impact on current industrial practice, and potential for use in future technologies. The articles selected include tutorials on asynchronous pipelines and synchronizers, case studies of successful chip designs and tools, and applications of asynchrony in emerging computing technologies. Contributions to this special issue were made by researchers from both industry and academia, and each article was selected through a rigorous review process.

The special issue starts with two overview/tutorial articles that provide fundamental background on circuit techniques for designing asynchronous and mixed-timed pipelined systems. The first article, “High-Performance Asynchronous Pipelines: An Overview” by Steven M. Nowick et al., provides an overview of pipelining in asynchronous systems. In clocked digital systems, CPUs and ASICs alike, pipelining has been the fundamental technique for decades to boost system throughput. This article
introduces the basics of several leading representative styles of asynchronous pipeline circuits. The second article is "Metastability and Synchronizers: A Tutorial" by Ran Ginosar. Metastability can arise whenever a signal is sampled close to a transition, leading to indecision as to its correct value. Synchronizer circuits must be used to protect against metastability, and their use is becoming ubiquitous with the proliferation of multiple timing domains on single chips. Despite the critical importance of reliable synchronization, this topic remains inadequately understood among many industrial designers.

The next three articles are case studies of practical chip designs and tools. They provide an excellent overview of the various levels at which asynchrony can be used with different trade-offs between performance, power, and design complexity. They range from the individual dynamic delay-insensitive gates of the first article, all the way to the globally asynchronous, locally synchronous (GALS) macroblocks of the third article. The first article, "Proteus: An ASIC Flow for GHz Asynchronous Designs" by Peter A. Beerel et al., presents an industrial-strength asynchronous ASIC CAD flow that enables the automatic synthesis and physical design of high-level specifications into GHz silicon, greatly reducing design time and enabling far wider use of asynchronous technology.

The second case study, "An Evaluation of Asynchronous Stacks" by Jo Ebergen et al., presents a fast and energy-efficient stack implementation. This design demonstrates two often-claimed benefits of asynchronous circuit design: the potential for high average-case performance and low power consumption. The third case study, "A Robust Architectural Approach for Cryptographic Algorithms Using GALS Pipelines" by Rafael Soares et al., presents the design of a cryptographic chip using a GALS design methodology. This design demonstrates the key advantage of using asynchrony in cryptography: the randomization of event timing internal to the chip leads to a dramatic increase in its robustness to side-channel attacks based on power and electromagnetic emission signatures.

Finally, two articles explore the potential role of asynchronous design in emerging computing technologies. In "Asynchrony in Quantum-Dot Cellular Automata Nanocomputation: Elixir or Poison?" Mariagrazia Graziano et al. compare the cost and performance of fully synchronous and mixed synchronous-asynchronous implementations of quantum cellular automata, and argue that asynchrony is inevitable at the top levels of QCA design. The last article, "Bringing Robustness and Power Efficiency to Autonomous Energy-Harvesting Microsystems" by J.F Christmann et al., introduces an architecture for a microsystem that is powered only by energy extracted from the environment to implement an autonomous sensing application. Key to this application is the use of asynchronous logic, which not only provides greater energy efficiency due to its event-driven nature but also, and more importantly, allows graceful adaptation to highly variable power availability.

**Asynchronous design has been, and continues to be, a wellspring of novel ideas for solving the next generation of microelectronic design challenges.** Although fully asynchronous products have been brought to the market, another indication of the success of this field is the manner in which it has influenced synchronous design—for example, inspiring approaches such as clock gating, synchronous elastic systems, and GALS design. It is our sincere hope that this special issue will give readers an opportunity to learn more about asynchronous design, from basic circuit techniques to design tools, and provide a glimpse into the future applications of this exciting area of research.

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*Luciano Lavagno* is a full professor at Politecnico di Torino. His research interests include the design of asynchronous and mixed-timing circuits and systems; system-level design, hardware-software codesign and high-level synthesis of digital circuits; and design
Montek Singh is an associate professor of computer science at the University of North Carolina at Chapel Hill. His research interests include asynchronous and mixed-timing circuits and systems; CAD tools for design, analysis, and optimization; high-speed and low-power VLSI design; and applications to emerging computing technologies and energy-efficient graphics hardware. He has a PhD in computer science from Columbia University.

Direct questions and comments about this article to Luciano Lavagno, Dept. of Electronics, Politecnico di Torino, Corso Duca degli Abruzzi 24, 10129 Torino, Italy; luciano.lavagno@polito.it; or to Montek Singh, Dept. of Computer Science, Sitterson Hall, Room FB234, University of North Carolina, Chapel Hill, NC 27599; montek@cs.unc.edu.

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