A Message from the Chair

At the 2010 International Conference on Computer-Aided Design (ICCAD) in San Jose, California, the DATC and CEDA organized a workshop dealing with parallel programming for EDA. This topic is important and timely, as many CAD vendors and university research groups have embarked on a quest to leverage multicore machines to speed up EDA applications. The workshop was well received—about 30 attendees spent a full day listening to presentations and contributing their ideas on this topic.

The Massachusetts Institute of Technology’s Arvind gave an engaging keynote speech. He first reviewed the attempt on parallel programming during the 1980s, a revolution that failed because the performance offered by parallel machines simply could not match the exponential growth of microprocessor performance. Single-thread performance was growing at a fast-enough pace to satisfy most applications at the time. Now the story, however, is very different—single-thread performance is now growing at an anemic rate, and multicore machines are all we have. Parallel programming is today a necessity, not an academic curiosity. Arvind asserted that the wrong goal is to generate hundreds or thousands of threads to keep the maximum number of processors busy. The right goal is to use the minimum resources to deliver the required performance, and parallel programming should be based on well-defined modules and parallel composition of such modules.

Following the keynote, Rensselaer Polytechnic Institute’s Mark Shephard reviewed the many-faceted high-performance computing research activities in RPI’s Computational Center for Nanotechnology Innovations (CCNI). The activities include finite-element calculation of mechanical parts and human organs, solid-state physics calculations, TCAD, nanodevice simulation, lithographic simulations, and EDA tools. Shephard’s talk was complemented by a talk on Amazon’s EC2, in which Jinesh Varia talked about the benefits of cloud computing, its relevance to EDA, and the different offerings that Amazon provides.

In other presentations, Adrian Ludwin of Altera then drew on his experience parallelizing place and route for FPGAs to talk about the successes and pitfalls of parallelizing EDA applications. Heidi Thornquist reviewed the software package (Trillinos) developed at Sandia National Labs for large-scale circuit simulation. Vasanth Tovinkere then presented the tuning and optimization tools that Intel provides for efficient development of robust parallel programs. Following Vasanth, Tim Mattson, also from Intel, explained how parallel programming can best be developed using parallel design patterns. Bor-Yiing Su applied the patterns concept developed at the Parallel Computing Lab of UC Berkeley to architect and implement parallelization of a time-consuming portion of the analytical placer, NTUplace3, with an impressive increase in speed.

Then Patrick Madden, a parallel-programming critic in his own right, moderated a panel session on “Practical Experience with Programming EDA Applications.” We had invited technical leads from major EDA vendors and industry to talk about their hands-on trials and tribulations of parallelizing key applications for their companies. The panel was preceded by an enjoyable, and congenial, wine-and-cheese reception. During the panel, there was an exceptionally lively discussion between Magma Design Automation’s Patrick Groeneveld and MIT’s Arvind on the pros and cons of partitioning as a parallelization approach. The panelists were insightful as well as vocal about the subject, so much so that the hotel had to dim the conference room lights at 7 p.m. in order to move us out.
I am gathering the slides from the presenters and will have them posted to the DATC website. I will keep all of you posted.

David S. Kung
DATC Chair
Senior Manager, Design Automation
IBM T.J. Watson Research Center
914-945-3183
kung@us.ibm.com

Message from the Editor

Please visit our website at http://www.datc.info, which has links to all our phone meeting minutes as well as our Newsletter and many other topics. Please take some time to critique the site; I would love some suggestions.

Joe Damore
Newsletter Editor

Calendar
12th International Symposium & Exhibits on Quality Electronic Design (ISQED 2011)
14–16 March 2011
Santa Clara, California
http://www.isqed.org

Fifth ACM/IEEE International Symposium on Networks-on-Chip (NOCS 2011)
1–4 May 2011
Pittsburgh, Pennsylvania
http://www.nocsymposium.org

21st Great Lakes Symposium on VLSI Systems (GLSVLSI 2011)
2–4 May 2011
Lausanne, Switzerland
http://www.glsvlsi.org

44th IEEE International Symposium on Circuits and Systems (ISCAS 2011)
15–18 May 2011
Rio de Janeiro, Brazil
http://www.iscas2011.org

CONTRIBUTIONS TO THIS NEWSLETTER: Please send any contributions for this IEEE Design & Test newsletter to Joe Damore, 36 Hagan Drive, Poughkeepsie, NY 12603; phone +1 845 462 1364; fax +1 845 463 4311; joepdamore@aol.com.

Selected CS articles and columns are also available for free at http://ComputingNow.computer.org.

Call for Articles

IEEE Software seeks practical, readable articles that will appeal to experts and nonexperts alike. The magazine aims to deliver reliable information to software developers and managers to help them stay on top of rapid technology change. Submissions must be original and no more than 5,400 words, including 200 words for each table and figure.

Author guidelines: www.computer.org/software/author.htm
Further details: software@computer.org
www.computer.org/software

January/February 2011