A Message from the Chair

At the CANDE (Computer-Aided Network Design Committee) 2009 workshop, I gave a presentation on the looming crisis that faces the EDA and design community. The reasoning goes as follows. Design complexity is exponentially increasing—when I was in college, my PDA was a calculator that added and multiplied numbers; today the handhelds can run apps that help you lose weight. Technology nodes in the future are becoming more difficult to develop and leverage, as a result of lithographic challenges and an increase in variability. In order to keep up, design tools must become more sophisticated, which translates into an increase in runtime. In the past, the increase in runtime was mitigated by the doubling of single-thread performance every 18 months or so.

With the demise of frequency scaling, however, performance is now provided by leveraging multicore machines so that efficient parallelization of EDA applications is no longer an option. Design tools are definitely taking longer to run—what used to take minutes could take hours or even days. People are taking notice, but from my vantage point, I've observed that some are putting up with the increase as a reality of life. Since the enormous amount of legacy codes are challenging to rewrite from scratch, some CAD developers have been fixing the problem in a piecemeal fashion, hoping that would temporarily stave off the crisis. This resembles the frog in a pot of water that is being slowly heated to a boil. The frog is now feeling quite a bit of heat, and if some drastic measure is not taken, it will end up on some dinner table.

To address this Grand Challenge, Andreas Kuehlmann (Cadence Design Systems), the IEEE CEDA chair, and I are organizing a workshop on "Parallel Programming for EDA," to be collocated with ICCAD in San Jose, California, on 11 November 2010. The workshop will bring together experts from the design automation community and the parallel programming community to discuss the timely issue of parallelization of EDA tools. It will provide a forum for leading researchers from CAD, parallel programming, and high-performance computing to present their latest research, exchange ideas, and conduct brainstorming.

Computing platforms are central to parallel programming, so we have invited luminaries from the HPC centers and cloud computing to explain how EDA applications might be deployed. Circuit simulation and place and route are core algorithms in design automation; we have two practicing experts to share their insights on parallelization of these algorithms.

Parallel programming is intrinsically a difficult proposition, and most CAD developers are new to this arena. Several parallel-programming evangelists will be talking about parallel-programming paradigms and tools that enhance the productivity of the code developers.

We round out the workshop with a panel of CAD development architects who have parallelized key EDA applications to share their success story. The goal is to exit the workshop with new algorithms suited for parallelization, new paradigms on parallelization, and cross-disciplinary solutions that target the characteristics of EDA applications. Please save the date and actively participate in this exciting event.

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Message from the Editor

Please visit our website at http://www.datc.info, which has links to all our phone meeting minutes as well as our Newsletter and many other topics.

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Please take some time to critique the site; I would love some suggestions.

Joe Damore
Newsletter Editor

Calendar

24th International Conference on Architecture of Computing Systems (ARCS 2011)
22–25 February 2011
Lake Como, Italy
http://conferences.dei.polimi.it/arcs2011/

12th International Symposium & Exhibits on Quality Electronic Design (ISQED 2011)
14–16 March 2011
Santa Clara, CA, USA
http://www.isqed.org

44th IEEE International Symposium on Circuits and Systems (ISCAS 2011)
15–18 May 2011
Rio de Janeiro, Brazil
http://www.iscas2011.org

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