From the EIC

Increasing yield and reliability through postsilicon tuning

Many of the challenges facing IC designers today can be attributed to process variations, but the worst of these problems are exacerbated by the widespread adoption of low-power design techniques such as voltage scaling, gate resizing, and dual-V_T assignment. Yield and reliability are severely affected by die-to-die and within-die parameter variations. Moreover, temperature and voltage fluctuations, and aging phenomena such as bias temperature instability, hot carrier injection, and time-dependent dielectric breakdown add to the burden of designers and chip manufacturers. In recent years, designers have welcomed postsilicon calibration and repair as a practical remedial approach to enhance yield, ensure fault tolerance, and tune the performance of chips after manufacture.

Recent special issues of *IEEE Design & Test of Computers* have highlighted presilicon solutions for addressing challenges related to process variations. This special issue takes a broader view of possible solutions and provides readers with insights into what is currently being done (and what we can possibly do in the near future) after manufacture through postsilicon adaptation.

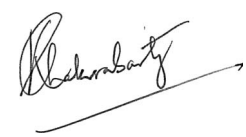
Guest Editors Swarup Bhunia and Rahul Rao have done an outstanding job in putting together this special issue with six selected articles, contributed by experts from both universities and industry. These articles cover research advances and practical experiences on a diverse set of topics, including mixed-signal and RF chip design, low-power SRAM design, memory repair in SoCs, predictive and statistical techniques to enhance yield, and system-level thermal management for many-core architectures.

Because the problems highlighted in this special issue are relevant to yield, reliability, and power consumption, the articles included here span both design and test aspects of chip and system design, and highlight the interplay between design and test solutions.

This special issue solicitation received many high-quality submissions; unfortunately, as a result of the tight review and publication schedule, we have been unable to accommodate all these papers in the special issue. Some of these papers are currently under revision for possible publication as articles in future issues of *D&T*.

I thank Swarup and Rahul serving as guest editors, the authors for their contributions, and the reviewers for their due diligence and adherence to the tight review schedule. I hope you will find this special issue useful and interesting.

On a personal note, this last issue of 2010 marks the end of my first year as EIC of *D&T*. I hope you have enjoyed the six issues of this year, and I look forward to serving you in 2011 with six more captivating issues of our favorite design and test magazine.



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