Next-generation design and test innovations

**Innovation is an** important differentiator in the semiconductor industry. Design methods continue to evolve to handle increased complexity, diverse functionality, and higher levels of on-chip integration. Advances in design technology and the scaling of semiconductor processes constantly motivate the need for innovations in test technology. This interdependence between design, manufacturing, and testing is becoming increasingly important as we tackle challenges related to yield, cost, and product quality.

This issue of *IEEE Design & Test* includes five articles that highlight the problems facing us with next-generation chips and systems. For instance, process variations are a serious concern for circuit design and performance estimation, and incremental timing analysis is prohibitively expensive for large designs. At the system level, task mapping must handle the dynamic nature of tasks in MPSoCs as well as address problems of network congestion in emerging interconnect fabrics such as network-on-chip. In testing, embedded test resources are increasingly being viewed as essential to reduce test cost, but ATPG methods require a language framework to describe these resources precisely and unambiguously.

The first article, “Measurement-Based Ring Oscillator Variation Analysis,” by Koh Jhoguchi et al., describes an analysis method, based on a surface-potential MOSFET model and the use of fabricated ring oscillators, for understanding process variations. Designers must accurately estimate, at a presilicon stage, intradie and interdie variations so that circuit delays and power can be accurately estimated and predicted.

“Speeding Up Physical Synthesis with Transactional Timing Analysis,” by David Papa et al., addresses the problem of carrying out incremental timing analysis efficiently in large designs. This article describes the use of transactional timing analysis, which avoids the need for significant timing calculations.

“Dynamic Task Mapping for MPSoCs,” by Ewerson Luiz de Souza Carvalho et al., highlights an important problem in system-level design. Many applications, such as multimedia and networking running on MPSoCs, involve a dynamic task workload whereby the number of tasks simultaneously running change with time, yet tasks must be mapped to the system processors to optimize various performance measures. This article shows how dynamic task mapping for such applications can be carried out in MPSoCs. An important objective is to reduce congestion in the network-on-chip interconnect fabric.

In “A Common Language Framework for Next-Generation Embedded Testing” by Michele Portolan et al., the authors describe a proposal for a new language that can describe embedded test resources in a chip for subsequent use by automated test generation tools. This language is positioned in the context of ongoing IEEE P1687 standardization activities.

The last article, “BIST to Detect and Characterize Transient and Parametric Failures” by Alodeep Sanyal, Syed Alam, and Sandip Kundu, describes a BIST solution to target circuit-marginality issues and soft errors due to single-event upsets. The BIST technique is useful for detecting faults as well as distinguishing intermittent failures from hard (permanent) failures.

Finally, after a long hiatus, we are glad to bring *D&T* readers a roundtable discussion in which experts debate and discuss the design of chips without hard guarantees on correctness of operation at all times.

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