From the EIC

Overcoming interconnect bottlenecks in gigascale ICs

INTERCONNECT COMPLEXITY is a serious problem for nanoscale ICs today, and this problem will only become worse as we continue to scale devices and integrate more transistors on a chip. Confronted by excessive delays on long wires and high power consumption, chip designers continue to wage a battle in the race against time for signal propagation, and to explore new solutions for interconnecting functional blocks.

Recent special issues of *IEEE Design & Test of Computers* have highlighted some of these solutions: for example, 3D integrated circuits, globally asynchronous and locally synchronous (GALS) systems, and network-on-chip. However, these approaches tackle the interconnect design problem from a system and architecture perspective, and because they are focused on making better use of copper-based interconnects, their effectiveness is limited by the bottlenecks inherent in the use of copper interconnects. Therefore, the need for new interconnect paradigms is being acutely felt today. As highlighted in the *International Technology Roadmap for Semiconductors*, there is clearly a tremendous opportunity to advance interconnect design by exploiting emerging nanotechnologies, as well as optical and wireless methods for on-chip communication.

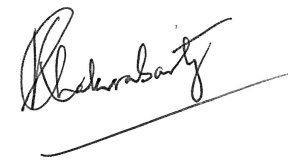
This timely special issue responds to this challenge by highlighting emerging and revolutionary interconnect technologies that can dramatically transform the way we design and fabricate ICs. Guest Editors Partha Pratim Pande and Sriram Vangal have done an outstanding job in putting together this special issue with five selected articles, contributed by experts from universities and industry. These articles cover research advances, practical experiences, and perspectives on future trends. Interconnects based on carbon nanotubes (CNT) and graphene nanoribbons (GNR), nanophotonics, RF—and a combination of CNT and RF—are described. These new interconnect technologies are especially exciting because they will facilitate the integration of heterogeneous, mixed-technology components in the same IC.

In addition to demonstrating high bandwidth, low latency, and lower consumption, experts also discuss issues of fault tolerance and manufacturability. Many of these emerging interconnect fabrics are highly susceptible to transient and permanent faults. The authors of the articles in this special issue explain how these challenges can be overcome and how we can design reliable interconnect architectures from inherently unreliable components.

The articles in this special issue are likely to stir a lively debate, as the design and test community understands and adopts some of these solutions, and delivers on the promise that is so evident today. How soon will these new interconnect structures replace today's dominant metal-and-dielectric planar interconnects? *D&T* is especially interested in this debate and follow-up articles from experts in the community.

The special-issue solicitation received a large number of high-quality submissions; unfortunately, due to the tight review and publication schedule, we were unable to accommodate all of them in this issue. Some of these papers are currently being revised for possible publication in future issues of *D&T*.

I THANK PARTHA AND SRIRAM serving as guest editors, the authors for their contributions, and the reviewers for their diligence and adherence to a tight review schedule. I hope you will enjoy reading the special issue.



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