FPGAs have been considered as possible implementation platforms for computation since the early 1990s. Over the technology generations, the regularity of FPGA designs has allowed them to stay at the leading edge of each new technology node, enabling their widespread adoption for embedded applications. The potential of FPGAs for scientific computation is well understood today; nonetheless, the long implementation cycles have hindered their faster adoption for numerically intensive scientific applications. We currently stand on a threshold, where various key research contributions and initiatives look poised to propel FPGA-based computation from the embedded space into scientific computing.

IEEE Design & Test seeks original manuscripts for this special issue, scheduled for publication in July/August 2011. The topics of interest include (but are not limited to) the following, as applied to FPGA-based accelerators with specific emphasis on challenges unique to scientific computing:

- Data representation for implementing fixed and/or floating-point arithmetic units
- Design space exploration, design languages, and hardware compilation
- Numerical analysis of FPGA designs and in-system validation
- Methodology case studies and comparison to competing high-performance computing platforms

**Submission and review procedures**

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to the IEEE Manuscript Central Web site at https://mc.manuscriptcentral.com/cs-ieee. Indicate that you are submitting your article to the special issue on "Design Methods and Tools for FPGA-Based Acceleration of Scientific Computing." All articles will undergo the standard IEEE Design & Test review process. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere. Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 References (30 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, logical organization, readability, and adherence to D&T and Computer Society style. Please see IEEE D&T Author Resources at http://www.computer.org/dt/author.htm, then scroll down and click on Author Center for submission guidelines and requirements.

**Schedule**

- Articles due for review: 15 November 2010
- Reviews completed: 15 January 2011
- Article revisions due: 15 February 2011
- Notice of final acceptance: 15 March 2011
- All materials due for edit: 15 April 2011
- Publication date: July/August 2011

**Questions?**

Please direct questions regarding this special issue to Guest Editors George Constantinides (g.constantinides@imperial.ac.uk) and Nicola Nicolici (nicola@ece.mcmaster.ca).