From the EIC

Enabling design and manufacturing through innovations in DFT

Testing and testable design continue to play a prominent role in the design and manufacture of ICs. New process technologies, higher chip complexity, and, increasingly, clock frequencies have led to a steady increase in test cost in recent years. Consequently, the semiconductor industry is especially concerned with managing test cost and ensuring product quality through advances in DFT, low-cost testers, and BIST. There is also an added emphasis on enhancing the value of test as a means to diagnose defects and increase yield. The interdependence between design and test is of paramount importance as we tackle pressing issues related to yield, cost, and quality.

This issue starts with a survey article, "Microprocessor Software-Based Self-Testing," by Dimitris Gizopoulos et al. Software-based self-test (SBST), a longtime active research area, is a promising technique to supplement functional and structural test methods. The tutorial provides a taxonomy of the different SBST methods that have been published in the literature, describes the role of SBST at various stages of microprocessor test and validation, and highlights recent trends and new directions.

The next two articles describe a wireless test platform that is being developed as a joint university/industry effort in Taiwan. In the first, "Economic Analysis of the HOY Wireless Test Methodology", Yu-Tsao Hsing et al. show that the HOY platform provides wireless test access and embedded design-for-test capabilities at lower cost and higher performance than conventional ATE. A test cost model is also presented to evaluate test costs for various manufacturing processes, and case studies are reported using the latest HOY prototype. Next, "Automatic Test Wrapper Synthesis for a Wireless ATE Platform", Ying-Yen Chen et al. describe the automated design of a test interface (called a test wrapper) and associated test programs for the HOY platform.

The next two articles, based on ITC 2009 presentations, address fault diagnosis and yield enhancement for the newest process technologies. The first article, "Feature-Ranking Methodology to Diagnose Design-Silicon Timing Mismatch" by Li-C. Wang et al., addresses the difficult problem of explaining the unexpected timing mismatch between simulation and measurement on fabricated chips. A kernel-based learning method is used to analyze and rank the design-related features that contribute most to the mismatch. In "Determination of Dominant-Yield-Loss Mechanism with Volume Diagnosis" by Manish Sharma et al., the authors present a volume diagnosis method to identify the root cause of yield loss. A statistical technique is used to analyze scan data and is combined with physical-feature data extracted from layouts.

The second part of a special perspectives article on the past, present, and future of EDA is also featured. This article reports on a July 2009 National Science Foundation workshop. The document is both retrospective and forward-looking, and it should especially appeal to the *Design & Test* readership. Part 1 of the report by Jason Cong and Robert Brayton was published in the March/April issue.

Finally, this issue includes two conference report briefs from Peilin Song, and from Adam Osseiran and Serge Demidenko. In Book Reviews, Scott Davidson examines *New Methods of Concurrent Checking* by Goessel, Ocheretny, Sogomonyan, and Marienfeld. This book describes various logic-level techniques for error detection and self-checking, especially for arithmetic circuits such as adders and multipliers. In a thought-provoking The Road Ahead column, Andrew Kahng writes about "More than Moore", functional diversification, scaling based on value and integration, and emerging technologies, drivers, and trends.

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IEEE Design & Test

 0740-7475/10/$26.00 © 2010 IEEE Copublished by the IEEE CS and the IEEE CASS