Guest Editors’ Introduction: Compact Variability Modeling in Scaled CMOS Design

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**PROCESS VARIATIONS IN SEMICONDUCTOR** manufacturing and their potentially negative impact on VLSI designs are well-known phenomena. Papers published in IEEE transactions and conference proceedings date back to the 1970s. Traditionally, variability has been considered a manufacturing problem in which the device and process engineers were supposed to minimize the variations. To guard against the impact of the residue variability, the designers were usually given a set of “corner” models in which the best- and worst-case models were specified.

As CMOS technology is scaled down into the nanometer range, variation control becomes much more challenging, having a fundamental impact on all aspects of IC design. Although continual improvements in manufacturing processes mitigate some of variability’s negative effects, the semiconductor industry is starting to accept that certain effects are better mitigated during the design phase. Handling variability in the design step will require accurate, consistent models of variability and its dependence on designable parameters, and of variability’s spatial and temporal distributions. Such models are quite different from the corner models deployed thus far to model manufacturing variability. Consequently, the compact modeling of systematic, spatial, and random variations is essential to abstract the physical-level variations into a format that designers can use.

With the support of the IEEE Electron Device Society, the ACM Special Interest Group in Design Automation, and the Semiconductor Research Corporation (SRC), we organized the first Compact Variability Modeling Workshop in 2008. The workshop’s goal was to bring together industry and academic experts with wide knowledge of device engineering, compact modeling, circuit design, and VLSI CAD so that they could address the challenges of variability. This special issue of *IEEE Design & Test* highlights, and expands upon, some of the presentations given at that workshop.

Process variations usually manifest as parameter fluctuations in a CMOS transistor. They are induced by the limits of either fundamental physics, such as random dopant fluctuations and line-edge roughness, or by the manufacturing process, such as the variability associated with gate dielectrics. As the minimum feature size is scaled toward 10 nm, both the amount of process variations and the sensitivity of circuit performance to variations are escalating. The first article in this issue, “Modeling Process Variability in Scaled CMOS Technology” by Samar Saha, reviews the predominant contributors of variations in sub-90-nm CMOS transistors. The article presents an overview of different modeling approaches (e.g., statistical corner model) that transfer the variability from the process domain into circuit simulation and the VLSI design environment.

At recent technology nodes, a major process variation is layout-dependent fluctuation from advanced manufacturing process techniques. The variations can result from sub-wavelength lithography, strained silicon engineering, and ion implantation, for example. These techniques enhance a CMOS transistor’s
nominal performance, but also introduce additional sources of variations related to layout nonuniformity. This type of variation interacts with layout parameters, posing further challenges to existing modeling and extraction methodologies. In “Layout Proximity Effects and Modeling Alternatives for IC Designs,” Xi-Wei Lin and Victor Moroz propose overcoming these barriers by model-based extraction that incorporates appropriate layout instance parameters into a compact device model. Such a solution improves the overall design turnaround-time and reduces the simulation cost.

In addition to layout-dependent fluctuations, a scaled CMOS transistor also suffers from many other random and temporal variations. A generic solution to achieve statistical design is to leverage standard compact device models, which are the interface between technology and design, and embed variations into a set of key compact model parameters. The accuracy of this approach, however, is affected by the specific model template, as well as by the extraction procedure from silicon data or TCAD simulations. The third article, “Statistical-Variability Compact-Modeling Strategies for BSIM4 and PSP” by Binjie Cheng and colleagues, calibrates the issues in statistical model parameter generation. By practicing BSIM and PSP extraction from 35-nm atomistic simulation results, the authors evaluate various statistical extraction methods.

Linking design and process, statistical compact models provide the essential correlation between performance statistics and process parameter statistics. The fourth article, “Extensions to Backward Propagation of Variance for Statistical Modeling” by Colin McAndrew and colleagues, features a method to systematically construct statistical models from measurement data. BPV uses the device behavior encapsulated within compact models to construct connections between the statistics of key circuit performance (e.g., saturation current) and the statistics of key process parameters (e.g., gate oxide thickness and effective channel length). The BVP method works well when linear correlations are assumed. An iterative approach is needed when nonlinear correlations are present.

At the circuit level, a digital microprocessor’s SRAM arrays represent the design most vulnerable to variations. For a planar transistor, the threshold voltage variations due to random dopant fluctuation and polysilicon gate line-edge roughness is making it harder to further reduce $V_{\text{min}}$ without sacrificing the stability of SRAM arrays. Designing SRAM with thin-body multigate transistors such as FinFET is a promising approach to mitigate this challenge. The last special-issue article, “Compact Modeling of Variation in FinFET SRAM Cells” by Darsen Lu and colleagues, describes a procedure to evaluate FinFET SRAM stability using an efficient FinFET compact model. The article also presents comprehensive stability analysis results, as well as a statistical design procedure for FinFET SRAM cells.

Increasingly, the consequences of process variation ripple throughout process development, device characterization, compact device modeling, and design strategy. At the device and circuit levels, understanding and successfully modeling the leading variation mechanisms is vitally important, not only to current robust design practice, but also to the prediction and management of variation levels for future IC technology.

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