Conference Reports

2009 IEEE European Test Symposium

ETS, held 25–29 May 2009 in Seville, Spain, featured presentations from 32 countries and 334 authors on scientific results, emerging ideas, practical applications, hot topics, and new trends in electronic-based circuit and system testing. One of the emerging topics presented was “TSV (Through-Silicon Vias)-Based 3D Stacked ICs.” New this year at the symposium was a PhD forum, which featured 12 students presenting their work in both an oral and a poster session. Winner was Piet Engelke (Albert-Ludwigs University). For a full report, visit http://www.computer.org/dt/conf_reports.

—Paulo Teixeira (INESC) and José L. Huertas (IMSE-CNM)

2009 IEEE East-West D&T Symposium

The 7th IEEE East-West Design & Test Symposium took place 18–21 September 2009 in Moscow, Russia. EWDTS was organized by the Kharkov National University of Radioelectronics and the Moscow Institute of Electronics and Mathematics. The presentations covered high-performance NoC, SoC, and SIP D&T; modeling and synthesis for embedded systems; system-level modeling debugging, and fault diagnosis; BIST and reconfigurable architectures; D&T for analog and mixed-signal circuits; and EDA tools for design and synthesis, among other topics. Sessions and interviews will be featured in a television program, “The Mirror of Science,” with leading western and eastern scientists. For a full report, visit http://www.computer.org/dt/conf_reports.

—Vladimir Hahanov, Kharkov National University of Radioelectronics

Panel Summaries

Predictive Solutions for Test—The Next DFT Paradigm

The basic approach to implementing test has been around for decades: logic is added to a design to enhance its testability and enable efficient pattern generation. This approach assumes the implementation results will meet designers’ quality and cost goals without impacting design functionality and performance. But with designs now routinely exceeding 10 million gates, test implementation is more challenging than ever. Can predictive solutions be used to efficiently implement DFT that meets all test requirements, given increasingly complex design timing, power, and area constraints? The test panelists presented their perspectives on the importance of predictable test outcomes and how predictive solutions might best be used to address the most challenging problems in test. For a full report, visit http://www.computer.org/dt/panel_summaries.

—Chris Allsup, Synopsys

Can EDA Help Solve Analog Test and DFT Challenges?

This ITC panel was organized by Ramyanshu Datta of Texas Instruments and Stephen Sunter of Mentor Graphics, and moderated by Carl Moore of Maxim Integrated Products. Carl asked about the challenges EDA companies face in developing DFT automation for analog/mixed-signal functions, the key issues for DFT and BIST, the solutions needed most urgently, and how effectiveness could be measured. One of the presenters emphasized the need for defect-oriented tests correlated to performance tests, so that the latter could be eliminated. An attendee questioned whether DOT could be accepted since it would mean companies wouldn’t directly test compliance with specifications. After the formal panel finished, a few panelists agreed to cooperate in proposing and developing an IEEE standard analog fault model. For a full report, visit http://www.computer.org/dt/panel_summaries.

—Stephen Sunter, Mentor Graphics

ITC 2009 Panels

Rohit Kapur, Synopsys

The ITC 2009 panel organizers summarize results for readers who could not be there in person.