From the EIC

**Welcome to the first** issue of *IEEE Design & Test* in the new decade. It is my pleasure to write to you as the new editor in chief (EIC). I am honored to succeed Tim Cheng and continue the tradition of excellence and service established by the former EICs. Under the visionary leadership of Yervant Zorian, Rajesh Gupta, and Tim Cheng, *D&T* has strengthened its position as the premier magazine for professionals, researchers, and students in the design, test, and design automation communities. *D&T* has also developed strong relationships with professional organizations such as the IEEE Test Technology Technical Council, the Design Automation Technical Committee, and the IEEE Council for Design Automation—and with major international events such as the Design Automation Conference, International Test Conference, and the Symposium on Integrated Circuits and Systems Design (SBCCI; Brazil).

During the past four years, I have served as a member of the *D&T* editorial board and I have had the honor of working closely with Tim Cheng on various aspects of *D&T* operations. I have been inspired by Tim’s vision and dedication to *D&T*, and I take this opportunity to thank him for his dedicated service and for setting such high standards.

I am pleased to inform you that Magdy Abadir has agreed to continue as associate editor in chief of *D&T*. Magdy is widely recognized for his excellent track record in industrial R&D and outstanding volunteer work for the technical communities served by the magazine. In addition, *D&T* will benefit from the continued involvement of past EICs (Yervant, Rajesh, Tim) in various advisory and editorial roles. In addition, I am also delighted to welcome several new members to the editorial board. They are listed in the masthead.

This issue of *D&T* includes five articles on the design of secure ICs and verifying the physical trustworthiness of ICs and systems. These timely articles address hardware security and trust issues related to threats such as malicious insertion of Trojans, intellectual property (IP) and IC privacy, and attacks designed to extract encryption keys. These security issues are especially relevant today due to the emergence of a globalized and horizontal semiconductor industry.

In the first article of this collection, Mohammad Tehranipoor and Farinaz Koushanfar present a survey of hardware Trojans, including a taxonomy and associated detection methods. The issue of hardware Trojans is examined for wireless cryptographic ICs in the second article by Yier Jin and Yiorgos Makris. The third article, by Kurt Rosenfeld and Ramesh Karri, describes security problems associated with the JTAG chain. It presents a protection and hardening scheme for JTAG based on lightweight cryptographic primitives such as stream ciphers and incremental message authentication codes.

The fourth article of this issue examines the problem of robust error correction, in which Meng-Day (Mandel) Yu and Srinivas Devadas explain how error correction is achieved with less information leakage compared to conventional methods.

IC piracy is a serious problem in today’s flattened IC supply chains. The reliance of companies on contractors, often offshore, has introduced security concerns related to piracy and IP protection. In the fifth article of this special issue, Alex Baumgarten et al. describe a metering technique to prevent IC piracy. The authors show how the standard design flow can be modified to intelligently place reconfigurable logic barriers in the chip.
In the “Guest Editors’ Introduction: Confronting the Hardware Trustworthiness Problem,” Mohammad Tehranipoor and Farinaz Koushanfar explain more about the special issue and provide additional detail concerning these five theme articles.

The final, nontheme article in this issue, “Verification-Purpose Operating System for Microprocessor System-Level Functions” by Lingkan Gong and Jingfen Lu, addresses system-level function (SLF) verification for microprocessors. It is difficult to run SLF verification on FPGAs since traditional FPGA verification involves the use of a general-purpose operating system. Gong and Lu describe a special-purpose operating system, VPOS, that can be used for SLF verification on FPGA prototypes.

Looking forward, D&T will continue to bring you state-of-the-art and practice-oriented articles. To achieve this goal, I rely on your regular feedback, submission of articles, and participation in magazine activities as volunteers. The forthcoming issues will continue to highlight roundtables, interviews, panel summaries, and articles on IEEE standards activities. In addition to providing coverage of mainstream topics, D&T will respond in an agile manner to the convergence of technologies (microelectronics, nanotechnology, IT, biotechnology, energy technology, etc.) and the emergence of new application areas such as green computing, renewable energy and energy harvesting, and cyberphysical systems. D&T will continue to maintain a vibrant editorial board consisting of active and visionary researchers and practitioners. Existing partnerships with conferences and professional communities will be strengthened, and new partnerships will be created to reach out to a wider audience. I am therefore excited by the opportunities that lie ahead and I look forward to working with all of you in taking D&T to new heights.

Krishnendu Chakrabarty
Editor in Chief
IEEE Design & Test

IEEE DESIGN & TEST EDITORIAL CALENDAR

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