From the EIC

Managing design and test challenges

Risks are notably increasing in the design of complex SoCs at the 65-nm technology node and beyond. Escalating design costs, increasing profitability and time-to-market pressures, and skyrocketing power consumption—in conjunction with a lower first-silicon success rate, and lower chip manufacturability and reliability—are among the key challenges that chip makers are confronting. To minimize the risks in the face of these challenges will require skillful management of the design process, which has become, not coincidentally, a core competency of leading chip makers. Design process management involves decisions to be made on both technology and business issues, and it also involves nurturing relationships with all the relevant partners in the chip design "ecosystem," such as third-party IP providers, EDA tool companies, design services houses, library vendors, and foundries. Critical decisions ranging from the definition of product features and specifications, choice of architectures and technologies, selection of partners, to the management and validation of milestones will have a tremendous impact on cost, time-to-market, and yield.

This issue of *Design & Test* features a theme on the management of emerging SoC development. The special issue consists of four articles, contributed by experienced design managers from leading semiconductor companies. In "The Story behind the Intel Atom Processor Success," Brad Beavers describes a new design that achieves a 10× reduction in power consumption. Andrew Chang's "Case Study of a 65-nm SoC Design" explains how MediaTek applied design strategies and associated methodology. In "From Specification to High-Volume Production," Manuel d'Abreu highlights SanDisk's experience, emphasizing design for manufacturability, of ramping up volume production for a new product. In "Low-Power Design Solutions for Wireless Multimedia SoCs," Jean-Pierre Schoellkopf and Philippe Magarshack describe a low-power design platform at STMicroelectronics. I would like to take this opportunity to thank our guest editor Yervant Zorian for the great job of putting together this interesting and unique issue.

In addition to these special-issue articles, you will also find four general-interest articles. "Incremental Verification with Error Detection, Diagnosis, and Visualization" by Kai-hui Chang et al. describes an efficient incremental verification system for physical synthesis optimizations. "Computing and Minimizing Cache Vulnerability to Transient Errors" by Wei Zhang introduces a new metric, the cache vulnerability factor, for measuring cache memories' susceptibility to transient errors, which enables cost and reliability trade-offs to be explored at the architecture level. "Hybrid BIST Scheme for Multiple Heterogeneous Embedded Memories" by Li-Ming Denq et al. illustrates a memory BIST architecture that minimizes routing overhead for designs with many embedded memory blocks. The last article, "Test Program Generation for Communication Peripherals in Processor-Based SoC Devices" by Andreas Apostolakis et al., discusses test program generation for SoC devices with embedded processors. The article demonstrates that communication peripherals in such devices can be effectively tested by the test programs generated by their hybrid scheme.

I hope you enjoy this issue. If you have any feedback, please share it with us.

Tim Cheng
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