Call for Papers

Special Issue on Design for Reliability at 32 nm and Beyond
Guest Editors: Yu Cao (Arizona State University)
Pradip Bose (IBM T.J. Watson Research Center)
James Tschanz (Intel)

VLSI design in the late CMOS era is driven by an ever-increasing challenge to cope with unreliable components at the device and interconnect level. Integrated circuit designers must comprehend emerging reliability issues at the 32-nm node and beyond to develop effective design and test solutions. Furthermore, designers must manage the impact of unreliability at various levels of the design abstraction—at the circuit, logic, microarchitecture, and system levels—depending on the nature and degree of errors that originate at the technology level.

IEEE Design and Test seeks original manuscripts for a special issue on Design for Reliability at 32 nm and Beyond, scheduled for publication in November/December 2009. This special issue will highlight the problem of design for reliability in the context of the emerging threat of progressively unreliable components used in the design of VLSI chips. Innovative techniques, which recognize the unique property of emerging reliability mechanisms and adaptively protect the system, are increasingly being favored in the design of high availability systems. Topics of interest include (but not limited to)

- Emerging reliability mechanisms
- Modeling and abstraction of new failure modes in scaled CMOS technology
- Error detection and correction
- Reliable circuit design and optimization
- Failure prediction
- Adaptive design techniques

Submission and review procedures

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to the IEEE Manuscript Central Web site at https://mc.manuscriptcentral.com/cs-ieee. Indicate that you are submitting your article to the special issue on “Design for Reliability.” All articles will undergo the standard IEEE Design & Test review process. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere. Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 150 words) and including a maximum of 12 References (50 for surveys). This amounts to about 4,200 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE D&T Author Resources at http://www.computer.org/dt/author.htm, then scroll down and click on Author Center for submission guidelines and requirements.

Schedule

- Submissions deadline: 1 May 2009
- Reviews completed: 30 June 2009
- Revisions (if required) due: 20 July 2009
- Notification of final acceptance: 31 August 2009
- Submission of final version: 20 September 2009

Questions?

Please direct questions regarding this special issue to Guest Editors Yu Cao (ycao@asu.edu), Pradip Bose (pbose@us.ibm.com), and James Tschanz (james.w.tschanz@intel.com).