The increased use of embedded predesigned reusable cores necessitates a core-based test strategy, in which cores are tested as separate entities. The goal of IEEE Std 1500-2005 (Standard Testability Method for Embedded Core-Based Integrated Circuits) is to simplify reuse and facilitate interoperability for testing core-based system chips, especially if they contain cores from different sources. The standard was developed over a period of 10 years, two years in a study group and then eight years in a working group—a long time, as is also alluded to in the Last Byte column of this issue of IEEE Design & Test. The reason for this long development time was that the stakeholders for the standard came from different industry segments. Consequently, there was a large, rather heterogeneous group of companies participating in the standard development working group: core providers and core users, integrated device manufacturers and fabless semiconductor houses, and EDA and ATE toolmakers. It simply took a considerable effort and corresponding time span to find a common solution that satisfied the heterogeneous requirements. The complete standard was first published in August 2005—now well over three years ago. Hence, it is a perfect time to present a status report on the usage and adoption of the standard, and that is exactly what the six articles in this special issue aim to do.

The first article, “IEEE Std 1500 Enables Modular SoC Testing,” written by the two guest editors, is a basic introductory-level tutorial on IEEE 1500. It also illustrates the standard’s usage through two application case studies, taken from chips designed and tested at the companies of the two authors.

Standards enforce a certain way of designing and testing, and hence are restrictive to total design freedom. Precisely for this reason, a standard is a great platform for an EDA company to build its tools on. The standard, set by industry specialists on behalf of a diverse set of companies, represents up-front market acceptance of the design and test practices it enforces. Tool support is also essential in the further proliferation and adoption of a new standard. Hence, it comes as no surprise that the next four articles all have strong links to the EDA community.

In “Improved Core Isolation and Access for Hierarchical Embedded Test,” Benoit Nadeau-Dostie, Saman Adham, and Russell Abbott present an EDA core-test approach based on the wrapper serial port (WSP) of IEEE 1500. Their core test wrappers reuse functional registers at the core boundary, thereby enabling at-speed testing and low area costs.

The next article, “Turbo1500: Core-Based Design for Test and Diagnosis,” by Laung-Terng Wang et al., describes a complete EDA tool flow based on IEEE 1500. As foreseen during the development of the standard, IEEE 1500 hardware interfaces with IEEE Std 1149.1 hardware at the SoC top level. The authors testify that IEEE 1500 helps contain the test and diagnosis complexity of large SoCs.

Next in line is “CTL and Its Usage in the EDA Industry,” by Rohit Kapur et al. This article gives a short introduction to the Core Test Language (IEEE Std 1450.6), which was codeveloped with IEEE 1500. The authors illustrate how CTL is used in EDA tool flows and how its usage could extend in the near future. Two sidebars in the article describe extensions to CTL: the Open Compression Interface and Memory CTL.

The following article in this special issue is “The ARM Cortex-A8 Microprocessor IEEE Std 1500 Wrapper,” by Teresa McLaurin, Stylianos Diamantidis, and Iraklis Diamantidis. It describes a methodology and associated tool for checking compliance with the standard, and uses a popular embedded microprocessor core as a vehicle to explain its technology.

The last article in this special issue is “Test Access Mechanism in the Quad-Core AMD Opteron Microprocessor,” by Kedarnath Balakrishnan, Grady Giles,
and James Wingfield. This article presents a true use case, in which a core-based test strategy fits very naturally with a multicore microprocessor. Taking IEEE 1500 as a given, the authors describe how they use the freedom and flexibility allowed by the standard to exploit the fact that their SoC contains identical cores.

**With these six articles**, our special issue is not over yet. We received so many strong submissions that *IEEE Design & Test* will publish more IEEE-1500-related articles in a forthcoming issue, as an overflow of our special issue. Keep your eyes open for those articles!

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