IEEE Embedded Systems Letters

CEDA currently publishes one transaction (IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems). T-CAD has seen significant increases in submissions over the past decade, requiring considerable resources to clear up the queue of accepted papers and improve turn-around time. Along with the IEEE Circuits and Systems Society, CEDA purchased an additional 50% of T-CAD’s budgeted pages in 2006 and another 20% in 2007, eliminated special issues, actively reduced acceptance rates, and decreased the maximum page limits on articles. Although these measures have reduced the backlog for articles in the queue from 14 months to about 4 months, it is ultimately limiting the extent to which we can provide a forum for publishing content related to embedded systems—an important part of CEDA’s scope.

We have been exploring various ideas for nurturing publications through which we can reach out to the community of embedded-systems researchers and provide an excellent outlet for timely dissemination of technology advances. To guide this effort and solicit community input, we formed an ad hoc committee about a year ago. This committee developed a proposal for a new journal, which was discussed by IEEE bodies in two phases. After an intense year-long effort by the ad hoc committee, the IEEE Technical Activities Board approved phase II in July 2008.

This new journal, called IEEE Embedded Systems Letters, will discuss the latest technical advances in embedded systems and related areas in embedded software. The emphasis will be on models, methods, and tools that ensure secure, correct, efficient, and robust design of embedded systems and their applications. CEDA will seek novel research papers in the following areas:

- embedded systems: architectures, automation algorithms, methods, and tools;
- microarchitectures, customizable processors, signal processing, multiprocessor SoC, and NoC architectures;
- VLSI and low-power design for embedded processors and systems;
- compilation and managed-runtime environments for embedded systems;
- profiling, measurement, and analysis techniques for embedded applications;
- design, specification, and synthesis of embedded systems: specification languages and models;
- hardware-software codesign, codesign methodologies, and design exploration tools;
- power-aware designs: modeling, analysis, estimation, and power management techniques;
- embedded-software design: models (programming models, formal models), methods, and tools for real-time and resource-constrained applications;
- programming languages and software engineering for embedded or real-time applications;
- testing, validation, and verification of embedded software;
- operating systems, middleware, and support systems for embedded-systems design;
- model-driven software design: formal models, calculus, and code generation;
- component modeling and component-based development methodologies;
- embedded control systems: design, analysis, and application to cyber-physical systems;
- embedded-systems security; and
- applications of embedded systems and software, including military, avionics, and automotive: case studies and applications of new methodologies and tools to applications with increased system heterogeneity and scale.

As with any emerging intellectual discipline, this journal’s areas of focus, special-issue highlights, and so on will evolve with important technical developments in the associated research communities. A particular strength of this journal will be its close association with research and practitioner forums.

Manuscripts for this journal should contain new results, ideas, or innovations that significantly advance the state of the art in embedded systems. They must not be submitted, accepted, published, or copyrighted elsewhere. However, because the intent is to quickly announce new results, more detailed versions of these
manuscripts may also appear elsewhere later. Each manuscript must be no more than four pages, or 2,200 words. The targeted publication time will be four months from the end of the month in which a manuscript is received, provided the author promptly responds to all communications and in accordance with instructions from the reviewers and editorial staff. To accomplish this goal, the outcome of the review process will be to either accept or reject each manuscript. Only minor modifications that do not warrant another review (other than by the associate editor) will be allowed.

Accellera: Paving the Way for EDA Standards

*The importance of standards to the EDA Community has motivated CEDA to work with the consortia and organizations involved in creating new EDA standards. Over time, CEDA hopes to present, in this newsletter, information about organizations that release and approve EDA standards. We begin with a discussion of recent efforts by Accellera.*

Accellera provides language-based design and verification standards for quick availability and use in the electronics industry. Along with its members, this organization cooperatively delivers much-needed open and practical EDA standards that lower the cost of designing commercial IC and EDA products. Because of Accellera’s partnership with the IEEE, Accellera standards are provided to the IEEE Standards Association for formalization and ongoing change control. Accellera’s board of directors includes representatives from ASIC manufacturers, electronics-system companies, and design-tool vendors. Most recently, Accellera released Verilog-AMS, Unified Power Format (UPF) for low-power designs, and Open Compression Interface (OCI) standards.

**Verilog AMS**

Verilog-AMS 2.3 encompasses and unifies analog and mixed-signal (AMS) extensions of Verilog AMS 2.2 (2005) to IEEE Std 1364-2005 (the Verilog hardware description language), which is widely used today for digital-circuit design and verification. Verilog-AMS 2.3 lets mixed-signal designers develop standard and tightly integrated Verilog-AMS modules, and lets EDA software tool developers implement EDA tools, without ambiguities in the language interpretation.

In addition to IEEE-1364 integration, Verilog-AMS 2.3 introduces new AMS features that enable improved top-down AMS design and verification methodologies. These include enhancements to common analog functions such as *table_models*, support for multiple analog blocks, and resolution of language conflicts with SystemVerilog IEEE Std P1800. The next phase of Accellera’s AMS technical activities will include integration of the AMS standard with the SystemVerilog language (IEEE Std 1800), and extensions to the AMS language for mixed-signal assertions and behavioral-modeling support.

**Low-Power UPF**

UPF for low-power design provides the ability to specify the supply network, switches, isolation, retention, and other aspects relevant to power management of an electronic system or electronic IP. The Accellera standard defines the relationship between the low-power design specification and the logic design specification captured via other formats (for example, standard hardware description languages such as VHDL, Verilog, and SystemVerilog).

**Open-Compression Interface**

Before on-chip scan compression, it was possible to use different design tools from different suppliers for test pattern generation and diagnosis. On-chip scan compression changed that model because each tool supplier offers a different type of scan compression logic and a tool-specific way to pass information between the insertion, generation, and diagnosis steps. The OCI standardizes how data passes from logic insertion to pattern generation, and from pattern generation to diagnosis.

After approval of the OCI as an Accellera standard, its adaptation as a broader, worldwide standard has continued under the IEEE P1450.6.1 Technical Working Group, thanks to the leadership of Bruce Cory, DFT Manager at Nvidia. (In fact, Cory was also the recipient of Accellera’s 2008 Technical Excellence Award for OCI leadership and contribution.)

For further information, please contact Yatin Trivedi (yatin@magma-da.com) or visit the Accellera website at http://www.accellera.org.

**Past Events**

**13th Si2/OpenAccess Conference**

13 October 2008  
Santa Clara, California  
http://www.si2.org/openeda.si2.org
Upcoming CEDA Events

CEDA conferences provide excellent opportunities for those interested in learning about the latest technical trends in electronic design and automation. If you’d like to participate or you have an idea about new topics of interest for our conferences, please contact William Joyner (william.joyner@src.org), CEDA vice president of conferences.

14th Asia and South Pacific Design Automation Conference (ASP-DAC)
19-22 January 2009
Yokohama, Japan
http://www.aspdac.com/aspdac2009

Design, Automation and Test in Europe Conference (DATE)
20-24 April 2009
Nice, France
http://www.date-conference.com

Great Lakes Symposium on VLSI (GLSVLSI)
10-12 May 2009
Boston
http://www.glsvlsi.org

7th ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE)
13-15 July 2009
Cambridge, Massachusetts
http://csg.csail.mit.edu/Memocode2009

45th Design Automation Conference (DAC)
26-31 July 2009
San Francisco

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