Guest Editors’ Introduction: Tackling Key Problems in NoCs

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Multicore chips are becoming common in industry, owing to increasing power consumption levels and raw-performance needs. This new paradigm places multiple cores on the same die and connects them through an on-die interconnect, effectively building a network on a chip. The NoC may interconnect identical or heterogeneous cores, depending on the application domain. Choosing the right design is extremely important because interconnects can consume substantial power and occupy significant real estate in silicon. Although multiple cores have started to appear in real designs, more sophisticated interconnects have only begun to surface recently in many-core chips.

Design and test methodologies for NoC design constitute a growing concern for future multicore and many-core chip designs. As Moore’s law enables trillion-transistor chips, and time-to-market pressures push designers to accelerate the design cycle, there is a critical need for CAD tools to help designers achieve NoCs’ tight power, delay, and area constraints with fast, correct designs. For example, tools for early design space exploration that would let designers trade off design considerations (power and area) with architecture requirements (latency and bandwidth) are sorely lacking. Synthesis tools that can handle heterogeneous cores and interconnect specifications while incorporating effects of the process technology accurately are only in their infancy stage. Verification and test of on-chip networks and their protocols, DFT and design for manufacturing (DFM) considerations, and back-end design methodologies targeting NoCs are other areas of potential research. This emerging research area also lacks a common evaluation standard and would highly benefit from the definition of a common benchmark suite.

This special issue highlights recent innovations in the design of such interconnects. The four articles fall into two main thrusts: the first three focus on design methodology challenges in NoCs; the final article demonstrates a practical case study implementation of an NoC.

“COSI: A Framework for the Design of Interconnection Networks,” by Alessandro Pinto, Luca Carloni, and Alberto Sangiovanni-Vincentelli, presents a software framework for communication infrastructure synthesis and optimization in distributed systems. Indeed, this is a very important problem as we move from a computation- to communication-centric design methodology for future electronic systems. Although the discussion is general, the authors illustrate the capabilities of the proposed framework for the synthesis of a communication infrastructure of multicore designs in which communication occurs via the NoC approach.

In “A Quality-Driven Design Approach for NoCs,” Stephan Bourduas, Jean-Samuel Chenard, and Željko Žilić present their early work in developing quality metrics to help designers make decisions about incorporating test, monitoring, and debug hardware in designs. Adding such hardware to reduce verification and test costs and using such metrics to guide architectural choices early in the design process constitute a promising approach to improving NoC design quality.

The next article is “Characterization of Equalized and Repeated Interconnects for NoC Applications,” by
Byungsub Kim and Vladimir Stojanović. This article focuses on the energy overheads of interconnects in NoCs and advocates leveraging equalization—a technique previously used for off-chip signaling—for on-chip interconnects in order to provide high-bandwidth, long-distance transmission. The authors propose a parameterized framework for modeling a wide variety of conventional repeated versus equalized interconnects, letting designers select the suitable signaling technique for their specific topologies.

In the final article, “An Interconnect Strategy for a Heterogeneous, Reconfigurable SoC,” Matthias Kühnle et al. present a case study of a chip prototype that demonstrates a reconfigurable NoC for a flexible programmable platform. They carefully provide details of this prototype, discussing the design choices made to allow scalability and flexibility across a range of applications in the domain. This prototype implementation sustains the required bandwidth for various application domains.

Although OCP-IP activities focus on multicore SoC development, its newest initiative targets the communication aspect of multicore design, which is closely related to the scope of this special issue. In the Last Byte, Ian Mackintosh, president and chair of OCP-IP, briefly introduces the OCP-IP NoC Benchmarking Working Group’s activities. This WG brings together various groups and research efforts in NoC benchmarking. Longer term, the OCP-IP initiative will contribute decisively to sharing benchmarks within the broader academic and industrial community.

**With increasing transistor budgets and multiple computing engines on die, it is imperative to move beyond bus-based and ad hoc network architectures to more sophisticated NoCs. Power-performance tradeoffs, IP reuse, and ease of verification and test are some of the primary design vectors for achieving a high-quality NoC design. Design methodologies and tools that facilitate design space exploration along these vectors must be developed and popularized. In the years to come, we hope to see mature research results in NoC design propagated from academia to industry, with sophisticated NoCs being a de facto component of many future multicore chip designs.**

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