IEEE/ACM MEMOCODE Contest Update

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The second annual IEEE/ACM MEMOCODE Hardware-Software Codesign Contest concluded successfully on 9 March 2008. This annual contest was conceived for the ACM-IEEE International Conference on Formal Methods and Models for Codesign (http://memocode-conference.com) to help highlight the issues distinct to hardware-software codesign and to expand the conference’s emphasis on design and practice. On 8 February 2008, a “secret” design problem involving the AES (Advanced Encryption Standard) algorithm and sorting was revealed on the contest website. Contestants were given one month to produce working hardware-software codesigned solutions, which would be judged on the basis of performance and elegance of design. Eleven finalists successfully completed the design, from 27 original teams drawn from diverse geographic regions in the US, Europe, and Asia. A panel of judges will evaluate the final design entries, with the winners formally announced at this year’s MEMOCODE, to be held 5-7 June 2008 in Anaheim, California, colocated with the Design Automation Conference (DAC).

This year’s contest is awarding two $1,000 cash prizes in the categories of the Highest Performance Design and the Most Efficient Design. In addition, Xilinx is sponsoring a special $1,000 cash prize for the best entry employing a high-level design methodology. Along with the three of us (who organized this year’s contest), the panel of judges also includes Kees Vissers (Xilinx) and Satrajit Chatterjee (Intel). This year’s contest is sponsored by Nokia, Xilinx, Bluespec, and CEDA. To see a description of the design problem and the contest rules, go to http://rijndael.ece.vt.edu/memocontest08. For more information, please contact Patrick Schaumont (schaum@vt.edu).

CEDA Honors Richard Brayton

CEDA is hosting a luncheon on 10 June 2008 at this year’s DAC to honor Robert Brayton, winner of the 2007 Phil Kaufman Award, for his impact on the field of electronic design through contributions in EDA. Brayton will give a lecture highlighting his career path and challenges, and will shed light on some of the turning points he has witnessed while working in industry and academia. In addition to this lecture, EDA award recipients (IEEE Fellow, IEEE Technical Field Awards, and so on) will be recognized for their accomplishments.

IEEE Annual Honors Ceremony

The annual Honors Ceremony, considered to be the IEEE’s most prestigious event, recognizes exceptional contributions that have made a lasting impact on technology, society, and the engineering profession. The program honors achievements in industry, research, education, and service. There will be 17 institute-level award recipients recognized at this year’s ceremony, which will be held on 20 September 2008 in conjunction with the IEEE Sections Congress in Québec, Canada.

This year’s IEEE Honors Ceremony is planned to start at 6:00 pm, with a dinner and afterglow reception immediately following. The event will be hosted by 2008 IEEE President and CEO Lewis Terman. The theme will be “Innovating to Meet the World’s Challenges.” All those attending the Sections Congress are invited. For further information, please see “Awards News” on the IEEE website or contact William Joyner (william.joyner@src.org).

Perspective: NoCs and EDA Tools Improve MPSoC Designs

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Many multiprocessor SoCs (MPSoCs) are used in devices where a low-energy operation of the system is critical. As technology advances, wire scaling is not on par with transistor scaling. Moreover, the number of communicating components in the chip, along with their speed of operation, is increasing. Because of these factors, the communication between the cores is causing a major bottleneck for system performance and energy consumption. With architectures becom-
ing more interconnect dominated, achieving an energy-efficient on-chip interconnect architecture tailored to the needs of the applications running on the chip is an important challenge that designers face.

In recent years, researchers have addressed this challenge in two ways: by developing methods and CAD tools to achieve an energy-efficient design and by developing scalable micronetwork-based architectures, or simply networks on chips (NoCs). CAD tools allow an exploration of the interconnect design space early in the design cycle and automate the building of efficient application-specific interconnect architectures. The NoC paradigm results in a structured, modular interconnect design with improved performance and energy efficiency.

The main goal is to let designers explore trade-offs in interconnect design—for example, between bandwidth, power, reliability, and area cost. State-of-the-art methods exist to solve some of the most important, time-intensive problems encountered during interconnect design, such as interconnect topology synthesis, core mapping, crossbar sizing, route generation, resource reservation, and RTL code and layout generation. Application-specific interconnect optimization can lead to significant improvements in all relevant cost metrics. Improvements by factors of 2 to 5 are not uncommon, and become even greater with technology and architectural complexity scaling. Design automation support is essential to guarantee that these custom-fit solutions can be readily deployed, tested, and verified. Although the state of maturity of these tools is not perfect, results are promising, and automated interconnect design is poised to become an essential component in energy-aware SoC design and validation flows.

Direct any questions and comments about this report to Srinivasan Murali (srinivasan.murali@epfl.ch).

Upcoming CEDA Events

IEEE CEDA currently sponsors or cosponsors 10 conferences and workshops, and two additional conferences in which it is in technical cooperation with other societies. Our conferences provide excellent opportunities for those interested in learning about the latest technical trends in electronic design and automation, and to be engaged with a community of volunteers. If you are interested in participating or have an idea about new topics of interest for our conferences, please contact William Joyner (william.joyner@src.org), CEDA vice president of conferences.

45th Design Automation Conference (DAC)
8-13 June 2008
Anaheim, California

8th International Forum on Application-Specific Multi-Processor SoC (MPSoC)
23-27 June 2008
Aachen, Germany
http://www.mpsoc-forum.org

3rd International Conference on Nano-Networks (Nano-Net)
15-17 September 2008
Boston
http://www.nanonets.org

18th International Workshop on Power and Timing Modeling Optimization and Simulation (PATMOS)
10-12 September 2008
Lisbon, Portugal
http://www.fpl.uni-kl.de/conferences/patmos/patmos.html

16th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC)
13-15 October 2008
Rhodes Island, Greece
http://vlsi.ee.duth.gr/vlisoc-2008

Embedded Systems Week (ESWEEK)
19-24 October 2008
Atlanta
http://www.esweek.org

IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
10-13 November 2008
San Jose, California

Formal Methods in Computer Aided Design (FMCAD)
17-20 November 2008
Portland, Oregon
http://es.fbk.eu/events/fmcad08

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