Personal computing systems and networking technology have evolved substantially over the years. These changes have dramatically affected the way we work, play, and socially interact. In particular, wireless technology has played an integral role in expanding the usefulness of our computing systems. Just consider how many features and functions are available on your cellular handset. We are truly in the age of mobile computing and network communications. The wireless technologies that have made the accelerated evolution in personal and mobile computing systems possible use RF integrated circuits. Today, very small, high-density RFIC chips are proliferating in application areas such as computers, consumer electronics, medical instruments, automotive applications, and military equipment. These RFIC chips enhance our everyday living by providing the portability and convenience we enjoy and have now come to expect.

RFIC evolution

Since the invention of the very first IC by Jack Kilby in 1958, it took about 40 years for RFICs to make their appearance in the semiconductor marketplace. Since the 1990s, there have been impressive breakthroughs in RFIC technology toward achieving high-performance, highly integrated RF subsystems. In early 2001, most researchers were focusing on the RF spectrum from 1 GHz to 5 GHz, while a few mavericks worked on RF circuits of up to 24 GHz. From a cost and integration perspective, CMOS technology has become an attractive process for manufacturing RFICs; however, SiGe (silicon germanium) and BiCMOS (bipolar CMOS) offer advantages over CMOS when it comes to certain aspects of RF power and performance. Today, researchers are working on millimeter-wave (60 GHz and beyond) RF circuits with digital CMOS technology for emerging applications in multimedia communications, personal-area networks, and automotive collision detection radar.

Challenges for RFICs

The future of RFIC technology is bright. However, there are several challenges (perhaps opportunities) in integration, performance, and cost for RFIC design and test. The demand in the wireless market will drive RFIC products. For RFIC chipsets, improvements are needed for the elimination of passive components, better integrated passives, power reduction, modeling of devices and interconnects, packaging, and cost-effective testing. However, this innovation cannot come at the cost of time to market for new products. Market windows for RFICs are shrinking, which places an additional burden on new product development engineers to accelerate product introduction cycle times. Additionally, development costs must be driven to a minimum, as average selling prices for RFICs remain flat or decline. Process technologies with SiGe, BiCMOS, GaAs (gallium arsenide), GaN (gallium nitride), and standard bipolar transistors are available for RFIC fabrications. However, cost-effective CMOS technology continues to amaze us with RFIC designs of up to 100 GHz. One of the biggest challenges in moving from low GHz to higher frequencies is the lack of integration between the production testing infrastructure, electronic design automation (EDA) tools, and device designs. Advancements in device and test equipment modeling and simulation technology are beginning to bridge this gap.

Additionally, RF measurement requires specialized capital equipment investments and highly skilled engineers with many years of experience. For example, RFIC noise measurements are highly sensitive and...
particularly difficult to perform on manufacturing-floor, production-test environments. Eliminating such tests by designing RFIC chips with built-in testability can potentially reduce or remove the need for specialized equipment and scarce engineering skills.

This special issue

The six articles in this special issue provide a wide perspective from academia and industry on the design and test of RFIC chips. We are especially pleased to provide articles from the semiconductor test industry.

Wireless technology is an essential part of RFIC design and test. In many RF systems, programmable filters are required to selectively reject certain frequency bands on the basis of various wireless standards. In “Design and Analysis of a Transversal Filter RFIC in SiGe Technology,” Vasanth Kakani and Fa Foster Dai present the design and analysis of a transversal RFIC filter. This 3.5-GHz notch filter provides a single-chip implementation using 45-GHz SiGe technology. The authors validate this RFIC filter by measuring the frequency response using a vector network analyzer. The integrated RF filter consumes 250 mW of power, with a total die size of just over 2 mm².

Ultrawideband (UWB) technology is emerging as a solution with low-power consumption and high enough data rates to be a viable replacement for USB (universal serial bus) cables, which have become ubiquitous for PC and peripheral connections. In “Design of a Low-Noise UWB Transceiver SiP,” Changwook Yoon et al. provide a complete solution for a UWB RFIC with a ball grid array (BGA) system-in-package (SiP) architecture. This architecture provides a complete solution for improvements in signal integrity, noise immunity, and reflection loss. The UWB transceiver SiP includes two semiconductor dies with passive bandpass filters and is compliant with US Federal Communications Commission (FCC) requirements.

Many heterogeneous SoC ICs with analog and mixed-signal (AMS), microelectromechanical system (MEMS), and RF subsystems cause bottlenecks in manufacturability, thus placing the entire production schedule in jeopardy. To avoid catastrophic delays, a new innovation in heterogeneous-IC testing is necessary. In “Decreasing Test Qualification Time in AMS and RF Systems,” Yves Joannon et al. describe a solution that uses design models and simulation testbenches to optimize test instrumentation use and thus decrease manufacturing test costs. Their test technique enables test hardware and software validation early in the RFIC design phase.

In “Light-Enhanced FET Switch Improves ATE RF Power Settling,” Joe Kelly et al. offer the perspective of a test equipment manufacturer providing practical, unique solutions for improving switching speed in RF switches. The authors use a high-intensity light source on RF switches to provide high switching speed. This switching technology on ATE provides fast settling times in RF sources, thus reducing test times by speeding up the overall RF test process.

Finally, because of schedule and space limitations, the remaining two articles for this special issue will appear in the March/April 2008 issue of IEEE Design & Test. The first of these, “Loopback DFT for Low-Cost Test of Single-VCO-Based Wireless Transceivers,” by Ganesh Srinivasan, Friedrich Taenzler, and Abhijit Chatterjee, discusses a loopback DFT test approach for RFIC chips that provides quick, economical test results at the wafer level. They show that test yield on the ATE for Texas Instruments’ RFIC devices exceeds 80% when this loopback DFT approach is used. The other article, “Wireless System for Microwave Test Signal Generation,” by Qizhang Yin, William Eisenstadt, and Tian Xia, discusses an RF embedded-testing technique that distributes RF sources to the chip via an antenna. The authors have demonstrated this technique on a 5-GHz low-noise amplifier (LNA), thus eliminating expensive RF probes and test fixtures.

RFIC chips represent the fastest growing semiconductor technology for computers, peripherals, multimedia communications, cell phones, and information technology. This IC technology will be lucrative for many sectors of the semiconductor industry. However, many challenges could delay advances in RFIC developments. This special issue describes some of these challenges and offers some solutions. We hope that these articles will help you to design and test further RFIC solutions that will meet these challenges and realize the tremendous potential of this promising technology.

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Kim has a BS from the University of California, Irvine, an MS from the University of Arizona, and a PhD from the Georgia Institute of Technology, all in electrical engineering. He is an associate editor of *IEEE Design & Test* and *IEEE Transactions on Advanced Packaging*, and the EIC of the IEEE Computer Society Test Technology Technical Council Newsletter. He is a senior member of the IEEE and the International Microelectronics and Packaging Society (IMAPS).

Craig Force is a senior technical manager and member of the technical staff in the Technology and Manufacturing Group at Texas Instruments, where he is responsible for technical and business strategies for RF integrated SoC design, simulation, and production test. His research interests include RF, analog and mixed-signal (AMS), and digital semiconductor manufacturing, test, and design development. His present focus is on the development and use of RF and SoC built-in test for reconfigurable design, validation, and production testability.

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