Greater accuracy and testability required for next-generation RFICs

Driven by the explosive growth of consumer wireless-communication applications, the design of low-cost, low-power, and highly integrated RFICs has made tremendous progress since the early 1990s. However, with the continued proliferation of new wireless standards, the drive for higher frequency, the demand for further integration of heterogeneous components onto a single chip or package, and the constant pressure on cost and power reduction, the design of next-generation RFICs remains challenging and demands innovation. In addition, with signal frequencies reaching tens of GHz, testing these circuits has created extraordinary challenges. Testing multiGHz RFICs requires complex signal generation and measurement. Moreover, this measurement often reflects a composite performance of the device under test, the equipment used to make the measurement, and the interconnections between them, as well as all the noise present in the entire testing environment. As a result, there exists no single test system that can economically and accurately test all of an RFIC’s specifications. DFT is essential, to address such test challenges.

The IEEE Design & Test editorial board has decided to run a special issue examining recent progress in, and future opportunities for, the design and test of RFICs. Our guest editors, Bruce Kim and Craig Force, have selected six articles for this special issue: four of them appearing in this issue, and two others appearing in the March/April 2008 issue. I would like to take this opportunity to thank Bruce and Craig for their great effort in putting together this special issue.

This issue of D&T also features an in-depth interview with Chris Rowen—founder, president, and CEO of Tensilica. D&T interviews editor Ken Wagner spoke to Rowen about the history of MIPS Computer Systems (a RISC processor company that Rowen cofounded back in 1984 and that was acquired by Silicon Graphics in 1992), his vision in founding Tensilica, and his perspective on the future of reconfigurable processors and multiprocessors.

Also included in this first issue of 2008 are four general-interest articles addressing diverse design and test issues. One of these articles demonstrates a scheme that uses a network-on-chip (NoC) communications infrastructure for high-speed delivery of manufacturing tests in multicore SoCs. Another article proposes a runtime power-monitoring scheme for embedded computing systems and demonstrates its application for dynamic power management. There is also an article that examines and quantifies the impact of bus layout, bus-coding techniques, and switching patterns on simultaneous switching noise. Finally, there is an article describing a software-based methodology for self-testing embedded processor cores. This methodology tests the core itself through execution of a synthesized test program. This article suggests a hybrid approach to test program generation using both deterministic and directed random approaches.

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