Combining synchronous and asynchronous timing schemes for high-performance systems

Clocks are an ever-increasing source of trouble. On the other hand, clockless designs would not likely be the solution for today’s or tomorrow’s monster chips, because of the immaturity of the design tools and the validation challenges caused by the subtleties of this design style. Globally asynchronous, locally synchronous (GALS) design, therefore, is emerging as the architecture of choice for certain applications. In a GALS system, the circuitry in each timing domain is locally synchronized, and different clock domains are glued together according to asynchronous communication schemes. This issue of IEEE Design & Test introduces some basic design and validation issues of the GALS architecture. Guest Editors Mike Kishinevsky, Sandeep Shukla, and Kenneth Stevens have selected five articles on this topic. These include a taxonomy on design styles, a survey of prevailing techniques and applications, a description of a GALS crossbar that uses token ring arbitration, a case study of a GALS infrastructure for a massively parallel multiprocessor, and an article on protocols for latency-insensitive design. The editorial from the guest editors outlines the scope of this special theme. I would like to take this opportunity to thank Mike, Sandeep, and Kenneth for their great job in putting together this strong issue. I trust you will enjoy reading it.

In addition to the special theme, this issue also includes a special section highlighting the International Test Conference (ITC). Guest Editor Anne Gattiker, the 2006 ITC Technical Program Chair, invited the authors whose papers were best received at ITC 2006 (based on both reviewer and audience ratings) to submit original papers for this special section. In this issue of IEEE Design & Test, they present updated articles on these topics beyond their ITC papers. After a rigorous review process, three articles were selected for this special section. One article presents a new test response compactor, whose strengths include the ability to handle a wide range of unknown (X) state profiles, a very high compression ratio, and excellent diagnostic resolution. Another article describes some of the debugging features of the Cell Broadband Engine that were added in this multicore processor to help debug unknown events. The last article enumerates some of the psychological factors that influence engineers’ decisions during design, DFT, and test processes. Better understanding of such factors would help foster better decision-making processes and, in turn, better designs.

Finally, this issue includes a short report of highlights from the 2007 Design Automation Conference held earlier this year. This report provides a short summary of the technical trends in this premier event on electronic design automation and silicon solutions. I hope you find it informative.

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