Supporting cost-effective innovation

In the nanoscale regime, speed and density of semiconductor technology continue to increase. However, skyrocketing design costs for developing gigascale system chips have effectively slowed the creation of new design projects. Such a trend could stifle further innovation and advancement in the semiconductor industry. A recent joint report from the Semiconductor Research Corporation (SRC) and the National Science Foundation (NSF), entitled Future Directions in Design Automation Research (http://www.src.org/member/sa/perspectives/corner/DesignAutomation_FinalReport.pdf) states the following:

There is a sense of urgency in the design automation research community today because the design methodologies and tools available to design the microsystems made possible by the continuing rapid advances in semiconductor technology cannot fully employ the technology in a cost-effective manner. Non-Recurring Engineering (NRE) costs associated with design are skyrocketing with estimates of over $30M per ASIC design undertaken. Moreover, the field of applications enabled by semiconductor technology is growing at a rapid rate ranging from very high performance microprocessors and signal processors to a broad array of low-power portable devices to micro sense/communicate/actuate networks of chips that are driven by very low per-unit cost and extremely low operating power.

To harness such new application opportunities, the semiconductor industry must expend more research efforts toward improving design productivity and reducing design cost. The industry can continue to blossom only if the trend of increasing design costs reverses and the electronic design infrastructure continues to support cost-effective innovation. If the design methodologies and tool suites can enable a team of 10 to 20 persons to design a system chip in 12 months, then surely more new startups in the area of chip design will spring up, with innovative product ideas to drive the industry forward.

Another key challenge associated with implementing gigascale system chips in nanoscale technology is that existing design and test solutions have not managed to address the increasing variability and reliability concerns. Variability can be induced by noise, process variations, thermal effects, and power-related issues. Among these, power-induced variations can wreak havoc on performance verification and delay testing in many ways.

In this issue, we examine recent progress in dealing with noise and variations caused by IR-drop and power supply noise (PSN) effects. Our guest editors, Mohammad Tehranipoor and Kenneth Butler, have selected seven articles from a large pool of high-quality submissions that cover the test, verification, and modeling aspects of IR-drop and PSN effects. I would like to take this opportunity to thank Mohammad and Ken for their excellent job in putting together this strong issue. In fact, we did not have sufficient room to accommodate the large number of high-quality submissions that cover the other aspects of this subject. So, we have accepted a few of these as general-interest articles, to appear in future issues of IEEE Design & Test.

I hope you enjoy this issue. If you have any feedback, please share it with us.

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