As the development costs and system complexity of integrated system on chip (SoC) continue to increase, the system-in-package (SiP) approach has emerged as an attractive contender for a wide range of applications such as wireless, sensors, graphics, and network packet switching. From a design and manufacturing point of view, SiP offers the flexibility of designing and fabricating each system component in its most appropriate technology—for example, using silicon germanium (SiGe) for high-speed logic, the memory process for DRAM, and a trailing CMOS technology with a larger feature size for analog components.

In principle, it makes great sense to design and fabricate smaller components with a high yield and integrate them into the larger unit—a principle that SoC does not follow. From the testing point of view, SiP could reduce tester costs; each type of part uses its own testers. In addition, components that can be repaired or reconfigured if defects are detected, such as memory, will not be burdened with defects in other parts that can’t be repaired, such as logic. Another great SiP advantage is integrating passive components directly onto the package substrate, which is an attractive feature for mixed-signal communication products.

Although successful and profitable applications have proven themselves in several market segments, significant challenges in SiP design and test remain for broader adoption. Currently, SiP design lacks an infrastructure. The enormous heterogeneity demands a unified design flow and a set of integrated tools that allow component and package codesign and cover electrical, functional, mechanical, and thermal analysis optimization. Because rework is costly, and thus not an option, the final SiP yield is proportional to the product of the individual good die yields times the package assembly yield. Therefore, SiP’s success will depend highly on the availability of the known good dies for heterogeneous components to enable high-yield system integration.

To take a closer look at these challenges and to examine emerging methods for addressing some of them, the IEEE Design & Test editorial board has dedicated this issue to SiP design and test. Our guest editors, Bruce Kim and Yervant Zorian, have done an excellent job in compiling six articles that cover topics from chip/package/system codesign flow and platforms to test needs and test flow to specific applications in high-speed serial links and cell phones. I thank Bruce and Yervant and all the contributing authors. I trust you will enjoy reading this issue.

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