TECHNOLOGY SCALING is moving high-performance ICs toward higher power dissipation, higher operating frequencies, and lower power supply voltages. As a result, power supply current through the on-chip power grid is increasing dramatically. In fact, the 2001 International Technology Roadmap for Semiconductors lists this as one of the key challenges facing the semiconductor industry. Several major industry players have stressed the need to better understand and control the power dissipation and power delivery aspects of ICs. For example, at the 2002 International Electron Devices Meeting (IEDM), Intel cofounder and Chair Andrew Grove said that power consumption is “becoming a limiter of integration.”

The reasons for the increase in chip power concern the manner in which the semiconductor industry has been scaling lithographic dimensions, MOSFET threshold voltages, and power supply voltages. If current trends continue unabated, microprocessors will eventually have the same power density as the wall of a nuclear reactor—they have already surpassed that of the common household iron. It is not uncommon to hear about a microprocessor with a 300-mm² area burning 150 watts! This special issue addresses the impact of this drastic increase in power consumption on current design practices, and specifically on the design and analysis of on-chip power distribution networks.

Power grid design

The design of appropriate power grids and the analysis of those grids’ impact on the timing and noise characteristics of a high-performance IC are crucial. Operating noise margins in modern designs are decreasing dramatically. Lower threshold voltages and the presence of many potential noise generators (usually caused by increases in signal-to-signal coupling in dense submicron layouts) eat away at the noise margins built into a design.

The power grid’s role is to provide the power (\(V_{DD}\)) and ground signals throughout a chip, with minimal impact on circuit operation. Because the grid inevitably has some amount of resistance and inductance, the supply voltage delivered to various parts of the chip will not remain constant, but will have a time-dependent variation caused by the switching of various functional blocks in the chip. Supply voltage variations can cause circuit delay variations, making the circuit slower than desired, or can even cause spurious logic transitions in extreme cases.

On-chip power grid analysis is difficult because the electrical models that represent the grid can be very large, easily reaching up to millions of components and nodes. Although similar problems occur in the analysis of large MOSFET circuits, there is a natural hierarchy and partitioning that lets us divide the problem into smaller components that are amenable to analysis. Power grids, on the other hand, are usually global across the entire design. Because they attempt to present as small a resistance between any given circuit and the power supply as possible, they are tightly coupled systems that allow no easy way for partitioning. This means CAD tools for power grid analysis lag somewhat behind tools used for circuit analysis, such as circuit simulators and static timing analyzers.

Recently, the growing importance of predicting power-grid-induced noise has led to a resurgence of interest in this area. Several conferences, such as the Design Automation Conference (DAC) and the International Conference on Computer Aided Design (ICCAD), have included excellent presentations on the topic. Moreover, IBM is releasing power grid benchmarks, which will be useful for developing and comparing alternative analy-
sis and design algorithms. Thanks to Sachin Sapatnekar’s generous support, these benchmarks, along with information on file formats and conventions, will be housed at http://www.ece.umn.edu/powergrid. Benchmarks are an excellent catalyst for engaging academia on cutting-edge industrial problems, but until now such benchmarks have been hard to come by in the area of power grid design and analysis.

This special issue

The purpose of this special issue is to further bring the area of power grid design and analysis to the attention of the design community. The issue includes five articles that address power-supply design and analysis, from the lowest chip-specific level all the way to links between microarchitectural design decisions and grid performance.

The first article, by Sapatnekar and Su, stresses the importance of building reliable power grids. The authors provide the basics of hierarchical analysis of power supply networks and address topology selection, wire widening, and decoupling capacitance insertion to optimize power supply networks. The authors highlight the need to simultaneously design signal, clock, and supply lines.

The second article, by Panda, Sundareswaran, and Blaauw, investigates the effects of low-impedance substrates on power supply integrity. The authors present a method to simulate the power grid and substrate for three designs, including a mixed-signal design. Their simulation results indicate the need to consider substrate effects while designing power distribution networks.

The third article, by Zheng, Krauter, and Pileggi, addresses the complex problem of modeling and analyzing massive 3D magnetic coupling in on-package power and ground distribution networks, typically containing thousands of conductors. Their approach, based on building detailed RCS and model order reduction (where $S$ represents susceptance), enables the efficient modeling of power and ground distribution networks.

The fourth article, by Mukherjee and Marek-Sadowska, looks at the impact of power grid noise on delay. The authors parlay a clever analysis paradigm into a method for reducing overall chip power by introducing clock gating at appropriate points in the logic.

The final article, by Grochowski, Ayers, and Tiwari, rounds out the power story by looking at the effect of microarchitectural decisions on power grid noise—specifically, noise related to the interaction between the chip power grid and the package.

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