The proliferation of electronic solutions in all aspects of life has dramatically increased, not only the number of embedded processors, but also the domains in which they reside. For example, nowadays, electronics consume a significant portion of an automobile’s cost. The mobile telecommunications revolution would have been unthinkable without the heavy use of embedded processors. Countless consumer electronics, from refrigerators to video games, rely on embedded processors.

This expansion in use, along with a dramatic increase in volume, calls for a reevaluation of existing embedded-processor models. The variety of dominant attributes—power in mobile applications, cost in automotive applications, reliability in critical aerospace applications, and performance in many other applications—impose significantly different requirements on the design and implementation of embedded-processor architectures. Whereas domain-specific designs promise an optimal fit to a particular application, general-purpose designs enable cost amortization across a significantly expanded base of applications and volumes.

The search for the right processor

As the embedded-processor marketplace searches for the appropriate processor model, designers are considering various candidate approaches. Perhaps the best-known example of domain-specific processors is the network processor. General-purpose microprocessors and microcontrollers still dominate the low end of the market. Attempts to capture the benefits of both domain specificity and generality now constitute a vibrant intellectual field, promising to inject fresh new perspectives into computer architecture research.

FPGA-based solutions provide generality at crucial design points. An alternative microarchitectural approach, enabling runtime incorporation of statically extracted application information, provides avenues for dynamic customization of embedded processors, while retaining fixed silicon amortization.

WASP 2002

The Workshop on Application Specific Processors, initiated in mid-2002, addresses the challenges of large, growing, yet diverse embedded-processor application domains and volumes. The workshop explores both research trends in academia and innovative applications and implementations in industry. It seeks papers on various approaches, which attendees can compare, drawing their own conclusions about which processor model is most appropriate. WASP encourages case studies so that attendees can see research principles in action and observe concrete data points.

WASP 2002 took place on 19 November in Istanbul, Turkey, in conjunction with the 35th Annual International Symposium on Microarchitecture (MICRO-35, held 18-22 November 2002), a premier symposium in the field of general-purpose microarchitectures. WASP attracted approximately 60 attendees, making it the most popular workshop at the symposium, and thus fostering a significant degree of interaction within the wider microarchitecture community.

Article submissions were impressive as well, with 32 submissions coming from a wide variety of locales. Slightly more than half the submissions came from Europe, a quarter came from Asia (evenly split between Japan and the rest of Asia), and the rest came from North America.

The program committee conducted a rigorous review process; each paper received an average of five reviews. The committee invited 19 of the papers for presentation at WASP, organizing them into four sessions.
network processors,
low-power architectures,
compiler support for application-specific processors, and
case studies.

A second round of reviews selected five articles that reviewers deemed worthy of publication in IEEE Design & Test.

This special issue

You will find the first four articles in this issue. Due to space limitations, the fifth article, “An Efficient and Low-Cost I/O Subsystem for Network Processors,” by Dionisios Pnevmatikatos, Ioannis Sourdis, and Kyriakos Vlachos, will appear in a later issue of IEEE Design & Test. These five articles represent a wide range of topics in application-specific processors.

The first article, by Raab et al., presents a case study on embedded-processor design in the automotive domain. The authors demonstrate the design and implementation of a next-generation, high-performance application-specific processor for vehicle vision systems. They propose an efficient architecture to fit the needs of the various applications related to driver safety and comfort in the automobiles of the future.

In the second article, Petrov and Orailoglu present a technique for embedded-processor microarchitectures that reduces power consumption on the instruction bus. The authors propose novel, low-power encoding based on functional transformations. They also introduce a dynamically reprogrammable hardware architecture that enables fixed silicon implementations.

The third article, by Lee, Choi, and Dutt, explores reuse maximization of memory references in reconfigurable processors with shared memory. It describes a novel compiler methodology for sharing memory bus interfaces among multiple processing units in a general, reconfigurable architecture. Efficient source-code-level transformations exploit the temporal locality across loop iterations.

The final article in this special issue, by Wahlen et al., provides techniques for retargetable compiler generation to accommodate various very long instruction word (VLIW) processor definitions. The authors propose a novel approach for automatic generation of a compiler’s instruction schedulers from the processor architecture description. This technique identifies VLIW packet instruction incompatibilities and, by using these relations, generates an efficient scheduler.

**WE HOPE** you find this special issue enlightening and informative. We thank Editor in Chief Rajesh Gupta, along with so many others, for making it possible. We thank the MICRO-35 organizing committee—particularly, General Chair Kemal Ebcioglu, who generously approved the collocation of the inaugural WASP workshop in conjunction with MICRO-35. We also thank all the program committee members, whose dedication helped in the difficult decision of selecting papers for presentation at the workshop, and in the even more difficult decision of selecting the set of articles for inclusion in this special issue. And last, but certainly not least, we are grateful to the many WASP attendees who, with their incisive comments, questions, and participation helped jumpstart a vibrant workshop.

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