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Program testing, cf. Formal verification.

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Pulse circuits, cf. Logic circuits.

Radio access networks
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Random-access storage
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Random-access storage, cf. DRAM chips.

Real-time systems, cf. Embedded systems.

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Research and development management
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Research initiatives
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formal verification of commercial ICs, Guest Editor’s Introduction, C. Pixley, July-Aug. 01, pp. 4-5.

Semiconductor device testing

Semiconductor storage
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large embedded memories, Guest Editors’ Introduction, R. Rajsuman et al., May-June 01, pp. 3-4.

Semiconductor storage, cf. Integrated memory circuits.


Showstoppers
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Silicon debugging, cf. Debugging.


Software design
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dynamic power management of electronic systems, Guest Editor’s Introduction, E. Macii et al., Mar-Apr. 01, pp. 6-9.
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formal verification of commercial ICs, Guest Editor’s Introduction, C. Pixley, July-Aug. 01, pp. 4-5.
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roadmaps and visions for design and test, Special Issue, Nov-Dec. 01, pp. 4-54.
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test trade-offs take center stage at ITC, Guest Editors’ Introduction, T. Ambler et al., Sept-Oct. 01, p. 59.

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Storage management, cf. Buffer storage.

Submicron defects
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Switching circuits, cf. Logic circuits.

Systems on chips
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SOC testability using LSSD scan structures, K. Zarrineh et
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June 01, pp. 56.
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Test strategies
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