Today’s microprocessors consist of tens of millions of transistors operating at extraordinarily high speeds. Test and verification of these high-performance devices continuously challenge engineers in every microprocessor design cycle. This special issue presents state-of-the-art techniques for microprocessor test and verification. It aims to provide innovative ideas and new methodologies to solve the difficult challenges facing engineers in microprocessor design environments, and to inspire further research activities regarding test and verification.

Realizing the importance of this topic, two workshops on microprocessor test and verification were organized as part of ITC week in 1998 and 1999. The workshops were quite successful in bringing together researchers from both test and verification fields to discuss the challenges and potential solutions. Several of the articles in this special issue have roots in one or both of the workshops.

This special issue contains seven articles that cover a wide area of topics. The first three articles can be classified as test articles. The first by Lai, Krstic, and Cheng discusses testing path delay faults in microprocessors. This has been widely recognized as necessary because of the type of defects observed in the fabs. Their method is based on the use of functional instruction sequences as test sequences. Under that assumption, they can demonstrate that a large percentage of paths are functionally untestable paths, leading to a reduction in the test generation effort.

The second article by Kranitis, Gizopoulos, Paschalis, Psarakis, and Zorian addresses the topic of reducing power during testing. They describe power/energy efficient built-in self-test (BIST) design schemes for processor data paths. An increasing number of industrial designs are adopting BIST to reduce the cost of test. The third article by Crouch, Mateja, Mclaurin, Tran, and Potter from Motorola describe the DFT features of a system-on-chip (SOC) design based on the Cold Fire microprocessor. The article describes the testability features of that design and many of the lessons learned by the team while dealing with the SOC test problems that are facing many engineers today.

The second group of articles in this issue cover various topics related to microprocessor verification. The first article by Utamaphethai, Blanton, and Shen addresses a method for measuring the effectiveness (coverage) of their microarchitecture test program generation within the buffer-oriented microarchitecture validation methodology. A list of design errors typically encountered in industry is used to measure the coverage. They propose the use of two metrics, functional deviation and timing deviation. Their simulation results demonstrate that their test programs detect over 98% of the errors based on the two detection metrics. This article demonstrates clearly how ideas from the test field, such as fault models, fault coverage, and so on, have influenced researchers in the verification area.

The second article in this group by Campenhout, Mudge, and Hayes also addresses
a topic relatively new in the verification field that has been influenced by test: design error models. The researchers analyze design error data that have been systematically collected over the last few years and report on lessons learned. The goal is to establish design error models that can be widely used to measure the effectiveness of various verification methods, similar to what is done in the test field using fault models like stuck-at transition delay, as well as others.

The third and last article by Krishnamurthy, Martin, and Abadir describes a validation methodology for embedded custom memories that is often found inside microprocessors. This validation methodology is based on the use of symbolic simulation. The article describes how this methodology was used to check the equivalence between RTL functional specification and the actual custom implementation of several complex embedded memories found inside some of the latest industrial microprocessors.

The final article in this special issue addresses a very important topic that is seldom addressed by researchers and practitioners: the topic of postsilicon validation. Post-silicon validation of microprocessors can consume as much time as the time spent on design. This is disturbing because of tremendous time-to-market pressures. Rotithor from Intel describes a systematic methodology for microarchitecture-focused post-silicon validation in the context of IA-32 Intel microprocessors. The article addresses many of the important issues to consider and many of the lessons learned.

By all means, it is impractical to address all areas in microprocessor test and verification within a single magazine issue. However, we hope that this special issue provides a good source for further references and future research. We thank all the authors and referees for their contributions in creating this special issue. We also express our sincere thanks to our colleague and friend Yervant Zorian for his support and guidance.

We hope this volume will satisfy your interest in microprocessor test and verification, and we hope it is fruitful enough to inspire more cross-area research to overcome future challenges.

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