A D&T Roundtable

Low-Power Design

D&T: We are still far from the power efficiency we need in our designs: a 100-times reduction. The semiconductor industry hoped to fill this gap using a multifaceted approach of reducing chip and package capacitance, lowering supply voltages, devising power management strategies, and using better design techniques and tools. What design paradigms really make sense for low power?

Meier: Designing for low power will require incremental changes in both design methodology and tools. Achieving our design goals will require designers to consider power throughout each design stage. One example is creating a typical simulation vector set that reflects system performance and the real power consumption of that design. As designers get some idea of activity information in their designs, they feed that information into power tools.

D&T: What tools will we need?

Meier: We'll need both new and existing tools to reduce power. Those tools will need to work within current design environments and follow the traditional design paradigm. However, the biggest problem we have today is evangelizing power awareness throughout the entire design community and encouraging change and adoption of incremental design methodology for power.

D&T: Do you see the design paradigm expanding?

Ko: Though there's no major design paradigm shift, it is expanding from the traditional trade-off between performance and area for IC design into an exploration of the three-dimensional space of performance, area, and power. So, it's another design constraint we must consider.
Clearly, there is value in low-power because things change as we go along. It may well end up radically different. For instance, at the expense of some acceptable silicon overhead and enhanced performance (which is the inverse of delay) per unit of power, we could reduce the energy consumption. Another approach is to increase the performance at a faster rate than power, as the overall design is still better off in energy efficiency. The winning solution is to improve performance at reduced power dissipation. This results in the most effective energy use.

However, today's engineers are under tremendous pressure, and the time to absorb new things is limited. Universities will have to play a significant role in helping designers understand the consequences of the steps to change, and low-power evangelists will have to encourage change. The major companies with the resources for strategic direction can map out where we're going. However, many design engineers just do it step by step, with the tools that are available right now because they just don't have the time to do a massive amount of work. They need help to do the next step, not next year's solutions.

For instance, at the operating system level and combinations and pulling together. What we have today in this area is certainly not design automation. I think we have some spot analysis things going on, a few techniques mostly based on voltage minimization.

D&T: What changes should be coming to reach the 100-times reduction that we really need?

Hines: One major change to get this reduction is a major paradigm shift. So we have to go out and look at the mechanisms. It's not just a matter of voltages; it's a matter of architectures, algorithms, and all of these things in combination and pulling together. What we have today in this area is certainly not design automation. I think we have a major task in front of us to get automation into this process.

Roy: I agree. We certainly have to change our overall design methodology for significant power reduction, consider the global view, and look at the different trade-offs and efficiency needs. We need accurate estimates of power dissipation, and our high-level tools are not yet that efficient. We also have to consider idle power management, which requires software control at the operating system level and complementary hardware features. We
should also provide for technology changes such as dual-gated SOI devices. These will require new design methodologies for circuit design and circuit level power management.

D&T: So, we need not only change in the existing methodology but also in development and experimentation with low-power design methodologies to determine the best one for the application that's intended. Now, let's turn to our design tools. What do we have now? What might we see in three years?

Meier: We have well-established transistor level analysis tools for measuring power late in the design cycle and for gate level analysis with tight links back to the HDL source code where designers actually enter the designs. We've seen announcements for short-term power analysis tools at higher abstraction levels.

D&T: Can you be more specific for the record?

Meier: There are simulation-based analysis tools that extract net toggle information to calculate power, like System Science’s PowerSim. Synopsys offers a higher level power analysis capability that uses probabilistic techniques and does not require gate level simulation. Synopsys supports a detailed gate level model that includes switching, internal, and leakage power. Accurate capacitance information annotation yields a good measure of power consumption in the design. In the near future, we will see gate level optimization tools that will automatically reduce the power in designs from the logic to the gate level. These tools will reduce power by 10 to 20% over current methods.

D&T: What can we expect in the longer term?

Meier: Tools will be available for analysis and optimization at higher levels of abstraction. Examples are high-level and behavioral-level optimizations in the synthesis flow. These tools will begin to incorporate power as a fourth dimension of the synthesis cost function, and will embed specific algorithms to perform automatic power reductions.

These tools will be very dependent on two things: One will be designer education on the importance of low power, and another will be their adaptability in incorporating power into their methodology. Designers will have to understand the environment, the system stimuli, and the power that their device consumes at these different abstraction levels. They will have to be intimately aware of these simulations and the toggle rates that tools are reporting. So, designers will have to make good use of these tools to achieve strong reductions in power.

Ko: As far as I know, vendors and universities are still in the early development stage with power optimization tools, though they're urgently needed. We can all learn from the performance bottleneck of today's analysis tools, and try to forecast for the next step of optimization tools. In 3 to 5 years, IC complexity could go up to 30 or 40 million transistors, and CAD vendors need to prepare to deliver tools for that kind of complexity with a reasonable performance.

For relative performance between various levels of power tools, I'd expect an order of magnitude speedup from one level of abstraction to the next higher level. For example, a power tool should be 10 times faster at the gate level than at the transistor level, and from gate level to RTL/architectural levels, an architectural tool should be 1,000 times
faster. A ±5% error at the transistor level is reasonable, and for each level higher, no more than two times the percentage in error margin.

**Napper:** It is a valid point to say that we’re still heading toward a brick wall in terms of the increasing complexity. But I do want to add a word of caution. The highly portable products and the microprocessor people are pushing the state of the art. They are already much more aware of problems and coming up with solutions. Others still face the challenge of gaining the knowledge and expertise in using existing tools.

Vendors have to service a very diverse market. One of our biggest challenges is educating engineers who are driven by project timelines. They’re in a project, they don’t want to listen, and they don’t want to know. So part of the solution is education, and vendors have to pursue successful strategies as well as solutions.

**Hines:** Our projections are generally low here. The R&D field has this term “gigascale integration,” which means not tens but hundreds of millions of transistors. Sematech’s projects, for instance, are driving toward this goal. We have to set those stakes in the ground, rather than some of these near-term goals.

I agree that today we are basically at the analysis stage. What we desperately need to do is think about a methodology in which to use these tools. What are we going to do with the analysis once we use these tools in our design process? What tools do we need to develop, and as we develop them, how are we going to use them in the design flow, and how would we integrate them into our overall environment? This is an extremely big issue, and at least right now, I just don’t see it being addressed.

**Roy:** We can achieve a large payoff by making the right architectural choices at the high levels of design abstraction. Universities and industry are addressing tools for low-power estimation and synthesis at the behavioral level. We also need efficient analysis tools at each design abstraction level for comparing two designs or making trade-offs. Absolute accuracy might not be all that important for designers in some cases, but our available tools are slow. Users want fast (within a few minutes for a 100,000-gate circuit) and fairly accurate (within 10 or 15%) power estimation tools.

**Meier:** Designers will require different performance and accuracy at different levels of abstraction. Early in the design cycle designers require efficient tools that provide rapid turnaround so they can evaluate design trade-offs and select the best architecture for a design. This is where existing probabilistic tools demonstrate good relative rather than absolute accuracy. Today’s tools won’t give us 100,000-gate analysis in one minute with 10% accuracy. Designers have to sacrifice absolute accuracy and use a relative accuracy number to establish these early trade-offs. Then, at least, they have some data to make design decisions and explore the design space. Later in the design cycle, absolutely, you have to iterate, and you have to verify. That’s where the more detailed, absolute-accuracy tools are essential in the design flow.

We haven’t mentioned physical design tools so far; they’re going to be important. Things like floor planners and place-and-route tools will have to take the power cost function into account. They will need to optimize the layout not only for area but also for power.

**D&T:** Any other comments about speed versus accuracy trade-offs for current and future tools?

**Hines:** Current tools are basically suited more for trend analysis than accuracy; they’re just spot tools to get us in the right ballpark. We desperately need a suite of tools and a methodology to go with them. We need a more graded progression of tool development with a stated purpose and goal in mind.

**Napper:** The design community has been remarkably adept at getting around its problems, even without the tools, figuring out solutions, and making things work. We’re not going to solve the far-out problems right away because we have a complex environment in which individual entrepreneurial skill, brilliance, education, and a variety of other things must coalesce to provide ways of going forward.

**D&T:** All right, achieving 100,000 gates per vector per CPU minute with 10% accuracy seems a very good target. It’s ambitious but not too farfetched, and we may have that capability in a year or two. Let’s turn now to what you see as the most effective approach for power minimization at the present time.

**Roy:** I see at least three promising approaches: scaling down the $V_{th}$ and the threshold of transistors, new circuit-level techniques, and technologies suitable for low power such as SOI. With near-IV supplies, circuit and architec-
Pedram: "... achieving 100,000 gates per vector per CPU minute with 10% accuracy seems a very good target. It's ambitious but not too farfetched ...."?

Hines: Certainly, most of the work today appears to be going on at the circuit level. However, the major gains are going to be at algorithm and architecture levels to minimize power. The voltage scale is going to contribute a factor of an order of magnitude, maybe a factor of 20, toward the 100-times improvement we need. The rest of the gains will have to come from architecture changes, such as new arithmetic structures, algorithms, and cell structures. That's where the largest payoff is going to be in the end.

Napper: I'm going to restrict myself to EDA tools. The new generation of both probabilistic and dynamic tools shows promise of being accurate enough to give designers confidence and also speed improvements. Designers are starting to measure power and understand it, and that logically feeds into wanting to move up just one abstraction layer to get faster, better, and earlier. Admittedly, it's still only analysis. Clearly, architectural analysis has the biggest payoff and will provide further insights to designers about the changes they can make and the rewards that they will get from it. However, it is still in a nascent stage.

Ko: There are a few options. One is doing nothing efficiently. This is more of a system power management approach in which we can suspend/shut down the whole system if no activity is detected, or power down specific units not in use. Another option is called energy-efficient computing. It involves the circuit, logic, architecture, and even software levels of power optimization.

D&T: Which will yield the most return?

Ko: The transistor or circuit level probably would yield up to a 30% return, and the logic level, probably 40 to 50% power reduction easily. Architecture should achieve 5 to 10 times power reduction. But let's not underestimate another important role software can play in energy-efficient data structure: compiler and applications. All of these contributors will come into play, and many disciplines will have to work together to accomplish true low-power design.

Meier: In the near term, the designer will achieve significant gains from a combination of advanced RTL source code improvements coupled closely with analysis tools, and automatic optimization. This approach will gain 40 to 70% in power improvements. Designers' modifications will bring this about, with good analysis tools that are tightly linked to their source. Designers will start to use this type of methodology in one to two years. In the longer term, I agree that the higher levels of abstraction and different circuit styles will provide some of the bigger gains.

D&T: What are the specific challenges that the design community must meet in the next two years or so?

Napper: Nailing down the accuracy-speed trade-off is a big challenge. Is 50% accuracy at 100 times faster acceptable, or 30% accuracy at 50 times? Designers will find one of these ranges useful or not useful because of the good or bad decisions they make based on the information they get back. For example, PowerMill has nailed the accuracy at the cost of speed, which means that it fits a certain application. Probabilistic analysis gives you substantial performance increases at the cost of some accuracy. Designers need to know that continuum to have the confidence to trust the tools and move forward.

Meier: I see two additional challenges. The primary one is really achieving the reduction that designers expect. John asks for two orders of magnitude; he needs basically an 80 to 90% power reduction. What we see today with automatic power optimization will give us 20 to 40%. So, there's a mismatch between expectations and what EDA tools can deliver. We can fill that gap through designer education and designer effort to adapt and use lower power design methodologies.

The second challenge is capacity. If we're going to have gigasize devices, today's analysis tools and runtimes won't be useful for fast iterations. Somehow, we need to break the capacity barrier so we can handle these design sizes.

Roy: It would be almost impossible to develop a "push-button" tool for this purpose given the state of the art. The best solution would be a tool to assist designers in assessing power and improving power requirements at every level. Another important issue is consistency between the estimation and analysis tools at various levels of design...
abstraction so different designs can be compared with high confidence.

**KO:** Let's not forget that in many applications the power tool needs to support a sign-off kind of accuracy before a design is taped out. Design and package engineers need to be assured that the device's power dissipation fits package constraint. So, at the lowest level of power analysis tools, we must have reasonably good confidence. In many cases, we would need an error margin of less than 5%. Yet, up to ±25% and ±50% of error margins at the RTL and architecture levels would still be acceptable during high-level trade-offs.

**D&T:** We also have to introduce low-power system synchronization approaches, the development and seamless integration of dynamic power management strategies, and power-conscious software techniques. How can we introduce these new tools, how quickly, and how can we make it as painless as possible for users?

**Hines:** The industry has begun to deal with issues like workflow managers from major players like Cadence, Mentor, and Intergraph. Properly used, these tools promise a degree of quick integration and seamlessness. Another factor that we haven't touched on is the need to develop standards for interfaces at the different levels; we need a concerted effort in this area. Also, interfaces in the CAD tool environments that some companies have will add to hierarchical types of environments. I've seen some good efforts there, though most are at low abstraction levels.

One impediment to seamlessness is that many high-level synthesis tools and data abstraction objects in the internal databases are driven by an RTL notion; we have to move into behavioral levels.

**Napper:** We have two major forces driving toward solutions. The design community, being a very active environment, isn't about to let anybody tell it what to do; it's going to tell the EDA community what to do. Also, we've shown over the last few years that our entrepreneurial system works and fosters creativity and new development. Other things will help smooth the transition: education—and the design community has to foster this—and standards

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**About the participants**

**John Hines** is chief of the Design and Modeling Branch in the Solid-State Electronics Directorate of Air Force Wright Laboratory, Ohio. He is the Air Force technical lead on the RASSP program and holds responsibility for several ARPA Low-Power Electronics technical base programs in the design area. He has been involved in computer-aided design development for 15 years.

**Uming Ko** is a senior member of the technical staff and the manager of the Low-Power Center of Excellence in Texas Instruments' Application Specific Products. His special interests include design techniques and methodologies for high-performance, low-power microprocessor development.

**Stephen F. Meier,** an R&D manager at Synopsys in Mountain View, California, has spent eight years in CAD development. His research and development group works on gate-level power analysis and optimization. He received his MS degree in electrical engineering from the University of California, Berkeley.

**Simon Napper** is vice president, marketing, at EPIC Design Technology, Inc., in Santa Clara, California. Previously, he was a marketing vice president at LSI Logic. He holds a BSEE from Brunel University in England.

**Massoud Pedram,** our moderator, is an associate professor of electrical engineering systems at the University of Southern California in Los Angeles. His research interests span many aspects of design and synthesis of VLSI circuits, with particular emphasis on layout-driven synthesis and design for low power. He received the National Science Foundation's Young Investigator award for 1994 and is the co-founder and general chair of the International Symposium on Low-Power Design.

**Kaushik Roy** is an assistant professor of electrical and computer engineering at Purdue University, West Lafayette, Indiana. His research interests include VLSI design/CAD with emphasis on low-power electronics, VLSI testing and verification, and FPGAs. He received a PhD from the University of Illinois at Urbana-Champaign and the 1995 National Science Foundation's CAREER development award. He is an associate editor of *IEEE Design & Test of Computers.*
"Another important issue is consistency between estimation and analysis tools at various levels of design abstraction...."

with cooperation between vendors. The design community has to insist upon these needs and be very realistic in its communications of those needs, or it will get the EDA vendors it deserves.

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