This issue of IEEE Design & Test of Computers is devoted to research and development in VHDL design automation. Two factors motivated the publication of this special issue. First, VHDL is rapidly emerging as a pervasive element in electronic product design; therefore, it is important that design professionals stay abreast of the language and its technology base. Second, several of the articles collected here are expanded versions of submissions judged to be the outstanding technical papers of the April 1991 VHDL Conference, sponsored by VHDL International. Their quality warranted disseminating them to a larger forum.

The first article, “VHDL: Toward a Unified View of Design,” presents an overview of VHDL. Coauthor Aart de Geus and I assess the maturation of VHDL by reviewing key historical developments. Then we discuss a variety of current VHDL research efforts, including data modeling, switch and analog modeling, performance modeling, and test modeling.

Two articles discuss VHDL synthesis. “DSS: A Distributed High-Level Synthesis System,” by Roy, Kumar, Dutta, and Vemuri, describes research being conducted at the University of Cincinnati to develop a high-level, distributed synthesis system. This work is investigating how to parallelize synthesis algorithms and how to use the concurrency in VHDL to guide the distributed synthesis process. “Specification, Planning, and Synthesis in a VHDL Design Environment,” by Nagasamy, Berry, and Dangelo, describes one of the first commercial efforts to develop an “industrial-strength” integrated design environment using VHDL and the results of high-level synthesis research.

Two articles discuss VHDL verification. In “Formal Verification of VHDL Descriptions in the Prevail Environment,” Borrione, Pierre, and Salem present an interesting alternative to simulation. Instead of using exhaustive simulation to prove that a VHDL specification and implementation are functionally equivalent, the authors’ prototype system uses theorem-proving and tautology-checking technology. “A VHDL Fault Diagnosis Tool Using Functional Fault Models” discusses an application of VHDL to testing technology. Authors Pitchumani, Mayor, and Radia have developed a design aid that uses the knowledge of the structure and behavior of a digital design modeled in VHDL to identify faults likely to be causing observed bad behavior.

This issue also contains part 1 of a group of short articles on various hardware description languages that have made seminal contributions to the present state of the art. Written by the original language designers, these articles provide an interesting look at how
the authors view their work in relation to the present and VHDL. The articles appear in the order in which the hardware description languages were introduced, as summarized in Figure 1.


The September issue will also continue the series on integrated diagnostics with Part 4, "Applying Testability Analysis Using an Integrated Diagnostic Framework," by John W. Sheppard and William R. Simpson.

Thanks to the efforts of the reviewers and contributing authors, we have an outstanding selection of articles, reflecting the rich history of hardware description language technology and the depth and breadth of VHDL research and development activities.

Figure 1. HDL timeline.

**TEST GENERATION DESIGN ENGINEERS**

We're developing the technology of tomorrow. You can make a significant contribution toward this effort at Amdahl today! Our world class organization is built on a solid foundation of people and their ideas, the ideas it takes to push information systems products and processes forward to the next step in their evolution. If you want to enjoy a technically innovative culture where individual contribution and teamwork add up to success, find out more about these exciting opportunities. We can't wait for the future, so why should you?

Intermediate to senior level positions exist for developing Automatic Test Generation (ATG) software and other design automation tools. You must have experience and extensive knowledge in the design and development of at least one of the following: delay test, function test, fault simulation, IDDQ testing, logic and timing simulation, and test generation algorithms. These positions require strong UNIX/C and software engineering skills, and a working knowledge of logic design, computer architecture and digital computer fundamentals. Familiarity with design for testability, BIST concepts, and GUI (X-Windows/Motif) is a plus.

To be considered immediately for your own place in the future, please call Susan Hubbart at (408) 746-6260, or fax/resume to Amdahl Corporation, Staffing Department AJL0503, 1250 East Arques Ave., P.O. Box 3470, Sunnyvale, CA 94088-3470. FAX (408) 746-8207. Principals only, please. Amdahl Corporation is an equal opportunity employer through affirmative action. All trademarks belong to their respective corporations.