GUEST EDITORIAL:

ITC 20TH ANNIVERSARY

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ITC 1989 Program Chairman

This special issue has its roots in the 1989 International Test Conference, which drew authors from around the world and technical papers on the cutting edge of electronic testing technology and all its relevant issues. The conference, which was held in Washington, DC, last August celebrated its 20th anniversary. Over the last 20 years, the complexity of electronic circuits, boards, and systems has increased dramatically, and the sophistication of testing techniques has been forced to keep pace. The International Test Conference is a well-established forum for test professionals to meet and share the latest developments in this continuing evolution.

In each successive year, the discipline of electronic testing becomes more complex, and its scope is also broadened. The ITC 1989 Program Committee received more than 300 technical papers on various aspects of testing, and over 100 of these were presented at the conference and included in the proceedings. Papers were selected for this issue of IEEE Design & Test to demonstrate the breadth and depth of test-related work first described at ITC 1989. In selecting the set of papers on which these articles are based, comments, ratings, and evaluations by conference attendees, program committee members, and outside testing experts were used. The authors of these articles have revised their papers to more clearly and completely present their technical accomplishments. Because of space limitations, numerous outstanding pieces of work could not be included, and I encourage you to investigate the entire conference proceedings.

The first two articles describe refinements to the tester hardware that advance the state of the art. "Integrating Tester Pin Electronics" is an example of the continuing integration of tester functionality for pin electronics. Such work reduces cost and increases both performance and flexibility by the use of modern IC fabrication technology. The author describes special new methods to overcome problems particular to such an approach—including automatic calibration and impedance matching. "Low Cost Testing of High-Density Logic Components" describes a new tester architecture that has been designed to match a novel testing method known as weighted random-pattern testing. The authors first describe several traditional testing methods—including metrics for their economic and logistical impact—and then demonstrate the superiority of the weighted random-pattern testing approach. However, the new method is viable only if the architecture of the tester used is appropriately matched to the testing technique. The authors describe modifications to an existing memory tester that match hardware and algorithm, and compare the costs of this new approach and more traditional testing methods.

The third article, "Built-In Self-Test of the Macrolan Chip," is an excellent example of a real chip design that includes special hardware to allow self-testing. Several novel observations and a thorough understanding of current built-in testing techniques are combined to achieve high-quality testing with a reasonable level of overhead in an IC circuit.
targeted for a real-world application—fiber-optic local-area-network communications. Several testing techniques are used, as appropriate, for different segments of the design, and the described engineering decisions serve as an excellent guide to others who might consider this type of testing solution.

The fourth article “A Testability Strategy for Silicon Compilers” describes high-quality work in one of the newer test-related areas. As design becomes more automated, it is important to consider the testing implications during design synthesis, and this article describes some of the most practical leading-edge work in that domain. The authors present a silicon compiler targeted toward digital-signal-processor designs with special emphasis on methods for introducing testability concurrently with synthesis.

Also included in this issue, but not originally presented at ITC 1989, is “Serial Interfacing for Embedded-Memory Testing.” The authors describe new design methods for testing embedded memories in application-specific digital ICs. Novel scan methods are combined with a study of pattern-generation techniques and the related hardware required for pattern generation. The trade-offs between more hardware (higher overhead) and better testing (detection of more memory faults) are explored and reported.

This special issue is my final task as program chairman for ITC 1989, and I would like to acknowledge the hard work and invaluable aid of many fine professionals. The aid and support provided by Ken Wagner, D&T’s editor for built-in self-test was invaluable, and the quality of this issue was significantly improved by his capable and generous efforts. I also thank the authors for their willingness to work under tight deadlines and their responsiveness to the suggested revisions and refinements.

The Steering Committee for ITC 1989 provided the multifaceted support that made the program possible. The ITC office handled mountains of paper, and to my knowledge, never dropped a pebble. The Program Committee for ITC 1989 met every single responsibility on time—even though the schedule was incredibly tight—and quality was never sacrificed for expediency. Finally, the authors, participants, and attendees at ITC 1989 individually and collectively played their appropriate part in a most successful, enjoyable, and informative exchange of information, discovery, and general good will. It was an honor and a pleasure to be associated with the entire event, and I anxiously look forward to ITC 1990.

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