Test bus interoperability

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A standard test and maintenance interface has been established as part of the Department of Defense’s submicron VHSIC program. The goal is to enable a subsystem comprising chips or chip-sets from multiple vendors to be monitored by a single (general-purpose) maintenance controller. The two-level, serial maintenance bus structure can be implemented in systems that use complex digital ASICs.

The submicron VHSIC contractors—Honeywell, IBM, and TRW—have defined both a chip and a board-level test bus to simplify on-chip interface circuitry and to reduce the number of drops on a single bus. These test buses are being implemented on numerous VLSI chip designs.

All three companies have prepared the test bus specifications with DoD direction. In so doing, they have achieved goals and requirements of the VHSIC program, and have recently turned the specifications over to the DoD for change control and distribution.

The two-level bus structure consists of the test and maintenance bus, or TM-bus, and the element test and maintenance bus, or ETM-bus, both of which are serial communications paths for the transfer of test and maintenance control and data information.

The ETM-bus uses simple, flexible bus protocol, allowing a small, vendor-specific ETM-bus slave interface to be implemented at the chip level. The TM-bus, on the other hand, implements a more powerful bus protocol that provides module-level test and maintenance control and monitoring.

The TM-bus could be used to interface to an ETM-bus controller when VHSIC chips are in the module, or it can provide interface capability to non-submicron VHSIC modules (see Figure 1).

The TM-bus is a multidrop bus that supports up to 32 slave modules residing on a single backplane. It consists of four signals: MASTER DATA—unidirectional, serial data signal from master to slave SLAVE DATA—unidirectional, serial data signal from slave to master CONTROL—bus control signal CLOCK—single-phase clock, max. 6.25 MHz CONTROL is used in conjunction with MASTER DATA to indicate the operational state of the TM-bus. MASTER DATA is also used to transmit messages consisting of a command header packet and optional data packets from the bus master to the slaves. The slaves use SLAVE DATA to transmit command and acknowledgment packets and/or requested data packets back to the master. All control and data transfer operations are synchronous with CLOCK.

The ETM-bus can be configured in either a ring or star structure and supports up to 32 slave elements. It consists of six signals: DATAIN—unidirectional, serial data signal from master to slave (star configuration) DATAOUT—unidirectional, serial data signal from slave to master (star configuration) SELECT—bus control signal MODE—bus control signal INTERRUPT—unidirectional from slave to master; signifies an error condition on slave SELECT, as its name implies, selects the appropriate ETM-bus slave for either instruction/status or scan operation, as determined by MODE. During instruction/status operation, the selected slave receives instructions over the ETM-bus serial data signals at the same time that it sends status back to the bus master.

When selected for scan operation, the slave routes serial data to the appropriate shift path on the chip as it sends the contents of the shift path to the bus master. When deselected, the slave executes the previously received instruction(s). All data transfer operations on the bus are synchronous with REFERENCE CLOCK.

For more information on the TM-bus and the ETM-bus or for copies of the specifications, contact J. Letellier, Naval Research Lab, Code 5305, Washington, DC 20375; (202) 767-2937.

**JTAG revised proposal**

The Joint Test Action Group has produced an updated version of its proposed standard implementation of boundary scan. Version 0.4 has been mailed to those on the JTAG European and North American mailing lists.

Anyone interested in receiving a copy of the revised proposal can contact the following individuals:

In Europe:
Colin Maunder, British Telecom Research Labs, Martlesham Heath, Ipswich IPS 7RE UK

In North America:
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