Spirited discussion at VLSI Workshop

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Active audience participation and, at times, even vigorous controversy, enlivened the Computer Society's VLSI Workshop, held in Clearwater Beach, Florida, February 22-25. The 50 attendees from academia and industry included professionals in different specialties related to VLSI design.

Topics of discussion included systolic architectures, residue number systems, circuit simulators, floor planners, multilevel routers, circuit analysis tools, verification strategies, design databases, and object-oriented design methodologies.

Some participants voiced interesting speculation as to the future of VLSI technology. Ron Young of Harris Semiconductor speculated that some form of doped aluminum would have to be discovered to replace today's conventional aluminum contacts. He further conjectured that four-level routing would become the industry standard in the near future.

Fred Taylor, from the University of Florida, Gainesville, gave an interesting report on the use of residue number systems for developing highly parallel computers. An advantage of this approach is that multiplication takes the same amount of computation time as addition or subtraction. While speed can be increased significantly by employing parallel processors, the difficulties of building the architecture for such a system might make it infeasible.

John Savage of Brown University described a device compiler capable of transforming high-level formal specifications into layouts. One attendee asked the obvious question: "Why another description language?" Savage explained that the lack of standardization in representation languages led to Brown's approach.

In CAD tools, Bill Heller of IBM emphasized the importance of floor planners in the chip design cycle. He argued that future floor planners will have to take multiple factors, such as timing, area, and accuracy, into account. M. Marek-Sadowska of the University of California at Berkeley described a global router for multilayer chip design. She argued that routers should consider the entire chip—not be based on graphs alone.

A top-down hierarchical method of segmenting the chip into vertical and horizontal sections, determining "holes" based on cut lines, and localizing the routing to these holes using a linear assignment algorithm was proposed.

Randy Bryant of Carnegie Mellon University described the COSMOS switch-level simulator, which has a goal of being 10 times faster than MOSSIM II. Ronald Rohrer of Carnegie Mellon presented the strategies being investigated to develop a circuit simulator several times faster than SPICE.

Advances in formal circuit verification were described by two participants: Daniel Weise of Stanford University and Nagendra Srinivas of AT&T Bell Labs. Weise's approach verifies MOS digital circuit behavior via automatic constraint extraction on the inputs. Srinivas' approach employs hybrid simulation and pattern matching to verify circuits at the logic level.

Several reports addressed systolic architectures. M. Chen of Yale University presented a method to transform simple configurations into directed acyclic graphs and to select an optimal or near-optimal configuration from these graphs. Bob Owens of Penn State University described how one could be "stingy" in designing multipliers to reduce the clock cycle requirements for the operation.

Jorge Aravenas of Louisiana State University presented a technique to iteratively perform computations using nonplanar interconnections of multifunction processing elements.

In other areas related to CAD, Steve Rubin of Xerox PARC described an electronic design database system that provides a homogeneous mechanism to define and propagate constraints up and down the design hierarchy; Bob Larson of Rockwell International presented an object-oriented symbolic editor; and J.A.B. Fortes of Purdue University described an expert system for design-for-testability.

This workshop did not issue a proceedings. Next year's workshop will be held in February 1988, chaired by Amar Mukherjee. C.K. Wong of IBM will be the technical program chairman. For more information, contact Mukherjee at Univ. of Central Florida, CS Dept., CC2, Rm. 205, PO Box 25000, Orlando, FL 32816-0001; (305)275-2345.

Kiawah Island BIST Workshop

Magdy Abadir and Jack Ferguson, MCC

Nearly 80 experts in BIST, half of whom are in US industry, gathered for the fifth annual Built-In Self-Test Workshop held March 11-13 on sunny Kiawah Island, South Carolina.

Marty Meth, deputy director of the DoD Weapon Support Improvement Group, began the workshop as keynote speaker, presenting several statistics on the test and maintenance problems in DoD. The numbers underscored the magnitude of the problem: 45% of the DoD budget goes to logistics and maintenance; 30% of the life-cycle cost of any system is for maintenance (excluding salaries); 20-40% of the defective components returned for repair are false alarms; and $5 billion is spent each year for related activities such as manuals and training.

The workshop comprised eight sessions of full presentations, eight sessions of mini-presentations, and several poster sessions and discussion groups. As is customary, almost every attendee was expected to give at least a mini-presentation. We have included a sampling of the more interesting presentations.

B. Krishnamurthy of Tektronix described a new graph-theoretic approach to fault simulation, in which pre-processing produces a graph whose nodes represent points of fanout and reconvergence within the circuit, and whose edges represent all paths between these nodes. For each pattern the graph is radically compressed, making fault simulation much simpler and faster than conventional fault simulation.

Two separate talks, by J. Waicukauski and by W. McAnney and J. Savir, all of IBM, addressed fault diagnosis when signature analysis is used. In Waicukauski's approach, the signature is monitored every 256 test patterns. If an incorrect signature is observed, parallel pattern, single-fault propagation is used to determine the set of faults that could have produced the observed test results.

McAnney and Savir's technique is limited to situations in which only one of the circuit response bits entering the
signature analyzer is incorrect. That is, only one test fails, and that test produces only one faulty output bit. The identification of the failed test (in a serial signature register, for example), or a short interval during which the failed test fails (in a multiple-output signature register, for example) can be quickly determined from the signature alone. Savir also discussed the outline of his forthcoming book on built-in self-test.

V. Agrawal of AT&T Bell Labs presented a mathematical model for estimating fault coverage for pseudorandom testing. Agrawal’s model uses a one-parameter family of curves to describe the profile of fault detectabilities (for random patterns). The one parameter can be estimated by curve-fitting the actual fault coverage obtained by fault-simulating a few test patterns.

Once the parameter is estimated, the fault coverage curve can be extrapolated to estimate the coverage to be provided by future test patterns. Agrawal also talked about extending the model to deterministic ATPG. In both cases, the model showed only a small error (2%-5%) in the prediction of coverage by future patterns.

Many who gave talks in the workshop expressed the need for integrated BIST solutions for system, board, chip, and subchip levels. Several presenters discussed standardized BIST interfaces. In addition, E. McCluskey of Stanford University stressed the need for a new set of benchmark circuits.

The Joint Test Action Group held an evening meeting open to all workshop attendees. The main goal of JTAG is to standardize boundary scan interfaces among European and US chip makers. The JTAG meeting was chaired by B. Curtois of IMAG in France.

The BIST workshop was created in 1983 to give participants a chance to talk about their work and the work of others in an informal, congenial atmosphere. It is a free forum for information exchange; the press is not invited, nor are tape recorders permitted. The 1988 workshop is scheduled for some time in March. Those interested can contact Richard Sedmak, Self-Test Services, 6 Lindenwold Terr., Ambler, PA 19002; (215) 628-9700.

Eric Rosenfeld of LTIX described the results of testing analog behavior using digital signal processing techniques. Complex analog test patterns are provided by a waveform synthesizer, and the device’s output waveform is digitized for computer analysis. Rosenfeld claimed that this approach produces results that are four times more accurate than analog methods, although he acknowledged that this approach cannot completely replace analog testing.

Jim Monzel of IBM described two methods for ensuring the performance of memories embedded in VLSI chips. In the first method, multiplexers and paths are added to make embedded memories directly accessible from a device’s inputs and outputs in the test mode. Two testers are required: a (slow) logic tester to detect logic and stuck-at faults, and a memory tester to evaluate dynamic memory performance.

In the second method, performance is assured through design and circuit analysis. The effects of all possible defects are analyzed, and the results are combined with defect distributions to project performance fallout.

Robert Rolfe and Signe Post from Harris described the TISSS tester-independent support software system. The software, under development at the RADC, translates test programs from various CAD systems to multiple ATE systems. A common database is created, and pattern files described in a subset of VHDL are one interface to the database.

Keiji Muranaga of Advansoft described a system called Advansite that enables waveform diagrams based on tester analyses, and other test-related information, to be graphically displayed on engineering workstations.

Several presenters discussed the future of large testers. The consensus seemed to be that relays will not be useful in testers operating at 100 MHz and above because of an impedance mismatch. A logical conclusion, then, is that dc and ac testing may not be possible on the same machine. The era of the general-purpose tester may be over.

For more information on the 1988 workshop, contact Mukund Modi, Naval Air Eng. Ctr., Dept. 52514, Lakehurst, NJ 08733; (201) 323-2560.