Physical Design of Microprocessors
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What is physical design? In VLSI, it is the task of implementing a desired logic into a marketable silicon chip package. Sounds straightforward enough, but actually exploratory development projects—without market goals—are much easier.

The development of marketable 32-bit VLSI microprocessor chips has to be done within strict limitations; be based on state-of-the-art technologies in silicon processing, testing, and packaging; and be accomplished on a very tight schedule. Add to that a constant push for more advanced CAD tools to accommodate innovative design approaches and you have something close to an impossible task.

Fey's statistical model for VLSI physical design effort reflects accurately the real-world design complexity. In 1984, it would have taken only about 20 man-years to develop a VLSI chip with 10,000 (nonrepeated) transistors, 20,000 PLA transistors, 8000 RAM transistors, and 50,000 ROM transistors—a sharp contrast to the much publicized silicon compiler's layout generation time of a few hours for low-end microprocessors.

Such a large gap clearly indicates that 'complete design automation' is not a reality at present. Moreover, it is highly questionable whether such a gap will ever be removed. Constant dialogue between CAD tool developers and physical designers is a good start at closing it, however.

It is this very problem that many of the designers in this special issue faced. In almost every case, CAD tools were stretched to the limit. Many other challenging aspects in the physical design of 32-bit microprocessor chips are also reported. I selected what I think is a representative set of state-of-the-art chips: AT&T CRISP, IBM Micro/370, Intel 80386, and two NTT 32-bit dedicated microprocessors.

In the first article, Dave Ditzel and Alan Berenbaum describe vividly how they solved many new challenging problems in the creation and integration of state-of-the-art CAD tools. H.H. Chao and his colleagues present an in-depth discussion on circuit and layout design for overcoming on-chip speed and noise problems in the second article.

The third article, by Pat Gelsinger, provides extensive coverage of design for testability and testing problems in the 80386 chip design. In the last article, Shoji Horiguchi and his colleagues from NTT show how VLSI processor chips were implemented using standard cells and three-layer metal interconnections. Their method achieved short design turnaround time, among other things.

The authors of these articles are to be commended. They are tireless champions who not only have survived all the ups and downs involved in a serious development project, but also have come forward to share their technical achievements for the design and test community.

Because of space constraints, we cannot possibly address all the issues involved in these types of projects, and so we have concentrated on the physical design alone. For those interested in project management aspects, I suggest Tracy Kidder's The Soul of a New Machine (Little, Brown and Co., 1981) and Frederick P. Brooks' The Mythical Man-Month (Addison-Wesley, 1982).

In the latter, Brooks poses and answers a compact question: "How does a project get to be a year late?—One day at a time." He must know well the daily stress VLSI developers go through to meet project goals.

Acknowledgments

I thank the following reviewers, in particular, who provided many constructive comments for this special issue: Prathima Agrawal, Vishwani Agrawal, Prith Banerjee, Wei-Tau Chiang, K.C. Chu, Al Dunlop, Kent Fuchs, and Ron Wadsack. Akihiko Yamada was very helpful in soliciting articles from Japan.

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June 1987

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