The Zycad Solution

Christine Miller, IEEE D&T

At the Automated Design and Engineering for Electronics (ADEE) West conference in Anaheim, California (March 31-April 2), Design & Test spoke with John Newkirk regarding the Zycad/Silicon Solutions merger of December 31, 1986.

Newkirk, formerly of Stanford University, is now both general manager of Silicon Solutions (a wholly owned subsidiary of Zycad) and executive vice president of marketing for Zycad. He described the merger as a pairing of two firms from different backgrounds producing basically complementary product lines—a supercomputer, off-the-shelf group in Minnesota and a designer of highly sophisticated VLSI devices, custom ICs and logic/fault simulators in Menlo Park. There is some functional overlap in custom design of small computers and large chips.

A "business as usual" approach is being taken by the two groups, with the added customer advantage of a broader array of mix-and-match products. Newkirk explained: "Basically, we sit down with the customer to find out what they're doing to determine what products they will need," adding that for items like analog-digital devices, users self-integrate the devices due to unavailability of turnkey products.

Newkirk predicted the ASIC (application-specific IC) market will become very large within the next two years, as parts become increasingly complex for board designers. Zycad's ASIC designer, Mentor, is targeted to fill the need of those who want a turnkey system with the speed of a turbocharger and transparency qualities.

Zycad is also adding behavioral level simulation to the LE (Logic Evaluator). Expansion of Silicon Solutions' Mach 1000 high-speed logic and fault simulation system is underway as well.

Although Newkirk was hesitant to forecast any development of merging product lines or other new products, he did refer to a possible joint marketing venture between Zycad and a vendor of analog tools.

New editors join D&T

Three new editors join D&T's editorial board. Miron Abramovici will be editor for Test Generation/Evaluation, replacing Edward McCluskey. Giovanni De Micheli replaces Don Thomas as editor for Synthesis and Verification, and Robert Powers takes over from Conrad Zagwyn as editor for New Products—Test.

Miron Abramovici, a member of the technical staff at AT&T Information and Communication Systems, brings to D&T his experience in logic and fault simulation, timing verification, hardware accelerators, design for testability, and test generation. Prior to work at AT&T, he was with the Department of Applied Mathematics at the Weizmann Institute of Science in Rehovot, Israel.

Abramovici received AT&T's Distinguished Technical Staff Award in 1986. A member ofEta Kappa Nu and a senior member of the IEEE, he holds an EE degree in applied electronics from the Bucharest Polytechnic Institute (1969) and a PhD in electrical engineering (computers) from the University of Southern California, Los Angeles (1980).

Giovanni De Micheli is assistant professor with Stanford University's Department of Electrical Engineering. Previously, he was codirector of the NATO Advanced Study Institute on Logic Synthesis and Silicon Compilation (1986); project leader of the Design Automation Workstation group at IBM T.J. Watson Research Center (1984); and assistant professor with the Department of Electronics at Politecnico di Milano. His research interests include CAD of ICs, with emphasis on automated synthesis, and optimization and verification of VLSI circuits.

He is coeditor of Design Systems for VLSI Circuits: Logic Synthesis and Silicon Compilation (Martinus Nijhoff, 1987). He holds a Dr.Eng. degree in nuclear engineering from the Politecnico di Milano (1979) and an MS and a PhD in electrical engineering and computer science from the University of California, Berkeley (1980, 1983). He has received many awards, including DAC Best Paper Award (1983) and Best Paper Award for papers published in IEEE Transactions on CAD/ICAS.

Robert Powers is product marketing manager for memory ATE systems at Teradyne. Prior to joining Teradyne in 1984, he worked at Dynatech Corp. as marketing and sales manager (1979); at Seaward International as a project engineer (1975); and at Exxon Production Research Co. as a research engineer (1974). He has seven years experience in marketing instrumentation and ATE and four years experience in project management and engineering.

Powers holds an SB and SM in ocean engineering from the Massachusetts Institute of Technology (1973, 1974) and an MBA from Harvard University's Graduate School of Business (1979). His editing and writing experience includes the preparation of numerous documents as part of his marketing duties, and his service as an editor of the yearbook and newspaper at Harvard Business School.

"D&T Scene" is continued on p. 62.

From left, Miron Abramovici, Giovanni De Micheli, and Robert Powers, D&T's new editors.
Memory component tester

The MS2300 from MOS Aid Systems is targeted for wafer probe and incoming inspection of SRAM, DRAM, PROM, EPROM, and EEPROM components. It features 1-ns timing resolution, 22 address lines (4M addresses), and data widths up to 8 bits (16 bits with a data multiplexer load board).

Capabilities include separate VIH/VIL voltage references for x and y addresses, data, and each clock; software address scramble; binary and gray code address sequences; and a range of test pattern and timing sequence selections. Built-in self-test diagnostics and autocalibration improve reliability and time.

A high-resolution PMU with relay pin matrix is included for dc parametric test and characterization. A mouse/graphics/windows-based software package eliminates user-written test software for almost all applications.

Typical MS2300 configurations cost from $95,000 to $125,000, depending on options selected. **RSN 16**

Multiple drive tester

The MDT-8000 multiple drive test system from Applied Data Communications can simultaneously test any combination of up to eight 5½” and 3½” drives through connection to one IBM PC or compatible.

The MDT-8000 consists of four or eight of the company's MD-506 hard disk drive testers connected to the PC through a proprietary asynchronous communications board.

Multifunction instrumentation system

Wavetek’s Model 680 multifunction instrumentation system houses up to eight high-performance instruments on a card in a single 7” high chassis.

Appropriate for military ATE, design engineering, and production testing applications, the Model 680 provides front panel or stand-alone operation with its menu-driven display. The system consists of a high-speed VME bus-compatible backplane, a VME main processor board with a 68000 MPU, 512K dynamic RAM, 128K nonvolatile static RAM, and 1024K PROM. It also has a reference/calibration board, a power supply, and up to eight plug-in instrument modules, including a 100-MHz pulse/timing generator and a 20-MHz arbitrary waveform generator/synthesizer.

The Model 680 uses a number of ASICs, such as a custom phase-accumulator chip, a custom counter chip, and a “divide by” chip.

Prices start at $30,000. **RSN 18**

Quadtree certification

Quadtree, the only simulation modeling company to obtain certification from the manufacturer of the digital devices it models, has a third certification agreement, this time with TRW's Electronics and Technology Division. Prior certifications were obtained from Texas Instruments and Weitek.

The TRW certification agreement calls for TRW to support and assist Quadtree's TRW VHSC Phase 1 model development activities and to certify that the models the company builds emulate the devices' functionality and timing.

Certification is the highest standard of accuracy used by industry to define levels of confidence in model performance. In many cases, certified models will be available even before device samples are available from the manufacturer.

Verification is the second highest standard of accuracy to define confidence in performance. In verification, the device manufacturer of the corresponding model provides the modeling company with detailed proprietary information concerning the modeled device, often including test patterns, but has not signed an agreement requiring that it state the models have been certified.

Validation is the third highest standard. Test vectors are used that were developed with expert understanding of the functions and timing characteristics of each device. Validated models are sometimes subjected to tests that use previously tested third-party software as an additional measure of accuracy. Validated models are then directly compared to the actual device using a hardware modeler.

GaAs contract

AT&T has been awarded a contract by the Defense Advanced Research Projects Agency to establish a pilot production line at its manufacturing plant to provide high-performance GaAs ICs to the Department of Defense.

The devices to be developed under the four-year, $19.8 million contract (which with options could total $30 million) will contain 3000 to 5000 logic gates per chip, operating in the 200-400 MHz range. Technologies to be used include selectively doped heterostructure transistor devices and enhancement/depletion circuits.

**D&T SCENE**

Continued from p. 8.