For the first time, you can test your VLSI prototype design at real world operating speeds. Thoroughly and easily. Across the entire cycle. Without compromise.

Topaz is a totally-integrated ASIC verification system that reduces prototype characterization and fault analysis time, while offering these exclusive advantages:

- **Full Data Formatting to 50 MHz** — for quick measurement of setup times and propagation delays.
- **256 I/O Channels at Speed, Without Multiplexing** — for maximum performance and flexibility.
- **Programmable Pattern Generation to 50 MHz** — for initiation of loops, branching and data control.

ASIC design requires painstaking accuracy. Verifying that design has been neither fast nor easy. The time available to get today's increasingly-complex ASICs to market continues to contract, and the price of an undetected error can be incredibly costly.

With Topaz, you'll know your design is right, and you'll know it faster. CAE-LINK™ software permits easy translation of simulator vectors into ready-to-use test vectors. And, our exclusive Meta-Shmoo™ software allows you to quickly sweep voltages and times at 500ps increments across an entire cycle, without programming.

It acquires data with a minimum of effort; and its ability to do graphic error-bit mapping and multi-level triggering gives it unequalled performance in failure analysis.

Topaz is a cost-effective solution to today's high speed ASIC verification needs, and the even higher speeds you'll require tomorrow. Call for complete details or your personal demonstration.

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